HP64000 Logic Development System

Model 64155A Wide Address Memory Controller

HEWLETT PACKARD

CERTIFICATION

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This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

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HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

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CW&A 2/81

SERVICE MANUAL

FOR

MODEL 64155A

WIDE ADDRESS MEMORY CONTROLLER

REPAIR NUMBERS

This manual applies directly to options with a repair number prefix of 2124A. For additional information about repair numbers, refer to options covered by this manual in Section I.

Manual Part Number: 64155-90901

Printed: June 1981

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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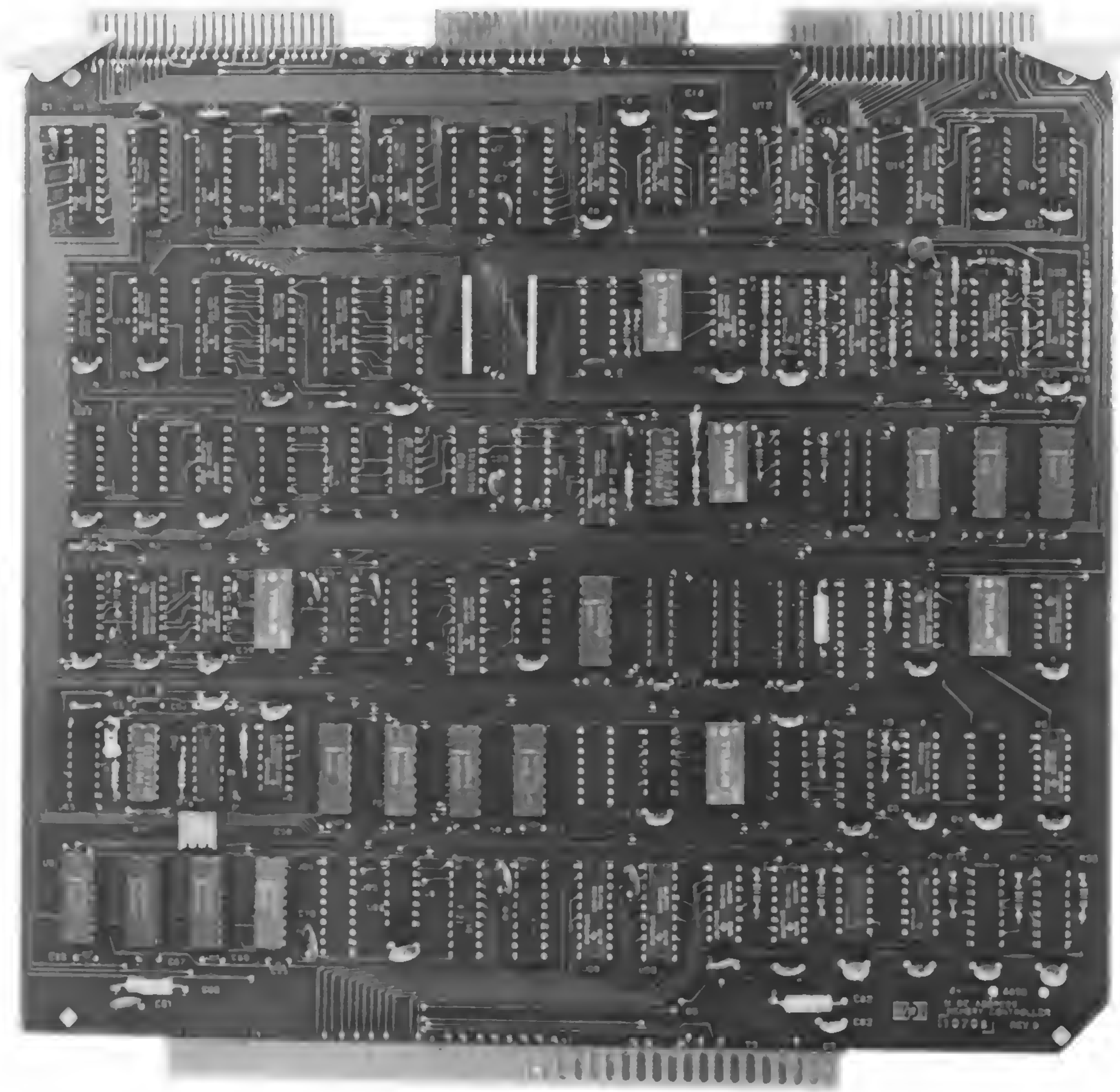


Figure 1-1. 64155A Wide Address Memory Controller Option

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual contains installation, replaceable parts, performance verification and service information for the Model 64155A Wide Address Memory Controller Option used in the HP 64000 Logic Development System.

1-3. OPTIONS COVERED BY THIS MANUAL.

1-4. The Wide Address Memory Controller Option is assigned a repair number which can be found on the printed circuit board in the following form: 0000A0000. It is in two parts: the first four digits and the letter are the repair number prefix; the last four are the suffix. The prefix is the same for all identical units and will change only if the option is modified. The suffix, however, is assigned sequentially and is different for each unit manufactured. This manual applies to options with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-5. An Option manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. An unlisted repair number prefix indicates that the option is different from those described in this manual. If this is the case, this manual should be accompanied by a Manual Changes supplement which explains how to adapt this manual for the newer option.

1-6. In addition to change information, the Manual Changes supplement contains information for correcting errors in this manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified by the manual print date and part number. Both may be found on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-7. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Sales/Service Office.

1-8. DESCRIPTION.

1-9. The 64155A Wide Address Memory Controller Option consists of a single printed circuit board which plugs into the Motherboard of the 64100 Mainframe. The 64155A is shown in figure 1-1.

1-10. The Wide Address Memory Controller Option is the interface between Emulation Memory, the installed Emulator and the 64000 operating system. It will also signal the analysis equipment and halt emulation when a GUARDED memory access is attempted and, if optionally configured, when a write to ROM is attempted.

1-11. This option maps the users address into available Emulation Memory. In a 16 Bit emulation system, up to four Low Power Emulation Memory Boards (HP Model 64152B, 64153B or 64154B) can be installed.

1-12. The Emulation Memory Address is specified via the data outputs of Mapper RAMs which reside on the Memory Controller Option. The Mapper RAMs also specify what type of memory the given block of Emulation Memory is supposed to act like (RAM, ROM or GUARDED Memory), or whether a given address is to be regarded as user address space and not acted upon within the Emulation Memory system.

SECTION II

INSTALLATION AND REMOVAL

2-1. INTRODUCTION.

2-2. This section contains information for unpacking, initial inspection, installation and removal of the Model 64155A.

2-3. UNPACKING AND INSPECTION.

2-4. Unpack the option and keep the shipping carton and cushioning material until the contents have been checked for completeness and the option has been checked mechanically and electrically. The electrical performance verification is given in Section IV. If the contents are not complete, if there is mechanical damage or defect, or if the option does not pass the performance verification, notify the nearest Hewlett-Packard Sales/Service Office. If the shipping carton is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard Office and keep the shipping materials for the carrier's inspection. The sales and service office will arrange for repair or replacement at HP option without waiting for the claim against the carrier to be settled.

2-5. INSTALLATION CONSIDERATIONS.

2-6. In a 16 Bit emulation system, up to four Low Power Emulation Memory Boards (HP Model 64152B, 64153B or 64154B) can be installed. Typically the Memory Boards are installed in Motherboard slots 2 thru 5 with slot 6 reserved for the Memory Controller. This recommended configuration is shown in figure 2-1. Notice that slot 9 is empty. This is to prevent accidental damage to Rear Panel Bus Cable which may occur if the board occupying slot 9 rubs against the cable as it is installed in or removed from the mainframe. If slot 9 is used, care should be taken when installing or removing the board to prevent damage to this cable.

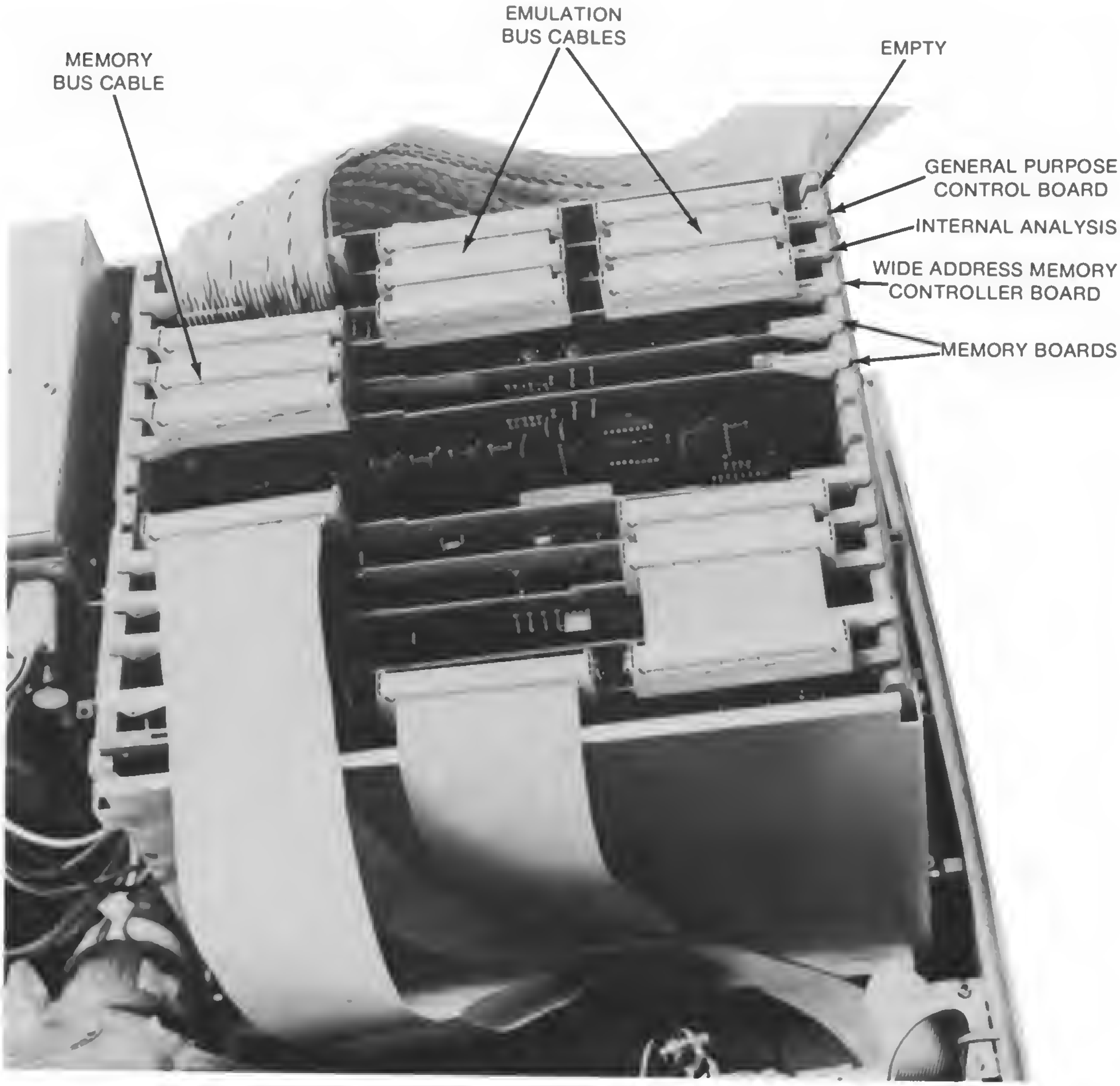


Figure 2-1. Recommended Motherboard Slot Configuration

2-7. SAFETY CONSIDERATIONS.

2-8. There are no high voltages on the 64155A Wide Address Memory Controller Board. There are, however, high voltages associated with the 64100 Mainframe and warnings are give where these voltages exist.

2-9. INSTALLATION PROCEDURE.

2-10. Use the following procedure to install Model 64155A.

a. Turn the mainframe power switch to the OFF position.

CAUTION

To avoid equipment damage in the following step make sure the component side of the Memory Controller is facing toward the front of the mainframe before the board is installed.

b. Orient the component side of the Memory Controller toward the front of the mainframe, align the edge connector of the board with the Motherboard connector and then press down.

c. Refer to figure 2-1 and connect the Memory and Emulation Bus Cables. These cables are keyed so that they can be installed in one direction only. Proper orientation can be verified by noting the orange dot on the left side of the cable connector when viewed from the front of the 64100 station.

d. Refer to Section IV and run the performance verification.

2-11. REMOVAL PROCEDURE.

a. Turn the mainframe power switch to the OFF position.

b. Remove the Memory and Emulation Bus Cables.

c. Pull up on the two extractor levers and remove the Memory Controller from the cardcage.

SECTION III

OPERATION

3-1. The functions of the 64155A Wide Address Memory Controller are transparent and require no interaction with the operator. Refer to the "16 Bit Emulator/Analysis Reference Manual" for an explanation of emulation and memory space partitioning.

SECTION IV

PERFORMANCE VERIFICATION

4-1. INTRODUCTION.

4-2. This section contains the performance verification procedures for isolating failures on the 64155A Wide Address Memory Controller and Memory Boards. The 64155A Wide Address Memory Controller is a blue stripe (exchange) item and not supported to component level repair.

4-3. Before attempting to isolate a suspected failure on the Wide Address Memory Controller Board, some preliminary steps should be performed to systematically isolate the problem. These are detailed in Section IV of the 64100 Mainframe Service Manual and summarized below:

a. Verify that the mainframe performance verification passes to insure that the problem is not in the mainframe.

b. Disconnect the target system to eliminate it as a possible source of the problem.

c. Reseat the Wide Address Memory Controller, Memory Boards and bus cables to insure good electrical connections.

4-4. PERFORMANCE VERIFICATION THEORY.

4-5. There are five individual performance verification tests that can be run. These include:

System -> Board Access Test

Memory Mapper Test

Memory Control Test

Memory Test

Emulation Access Test

4-6. The above tests can be run individually, or the tests can be cycled and repeated automatically. These tests and the procedures to run them are described in the following paragraphs.

4-7. To run the performance verification tests, it is first necessary to execute the option_test instruction. This instruction directs the 64100 to identify the option boards occupying its cardcage and then load the appropriate performance verification software. To do this, type in the following lower case instruction (figure 4-1):

option_test RETURN

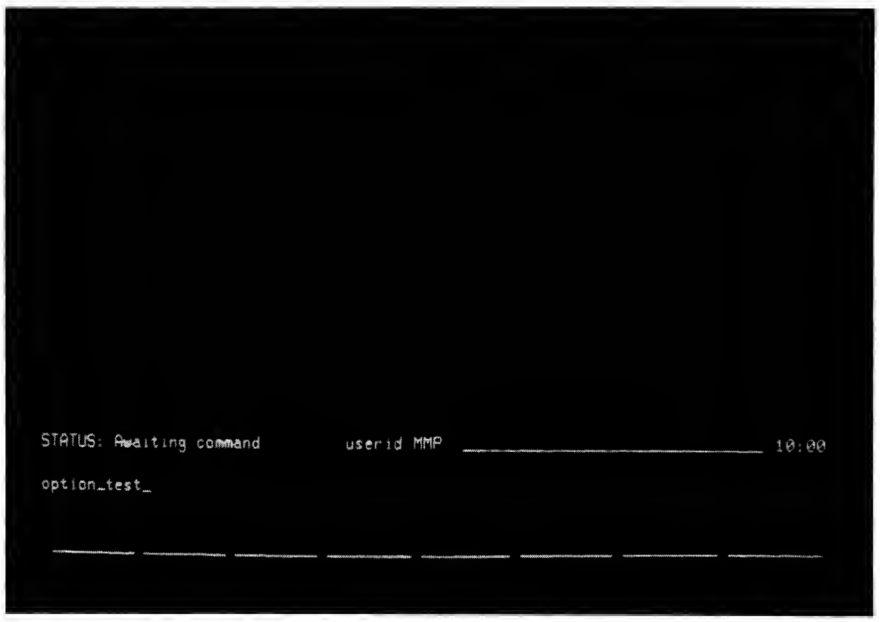


Figure 4-1. Selecting option_test

4-8. The CRT will now display a directory of the installed option boards with their corresponding slot locations. A typical example is shown in figure 4-2. Enter the slot number indicated for the Wide Address Memory Controller. For example, if the Wide Address Memory Controller is in slot 6, enter:

6 RETURN

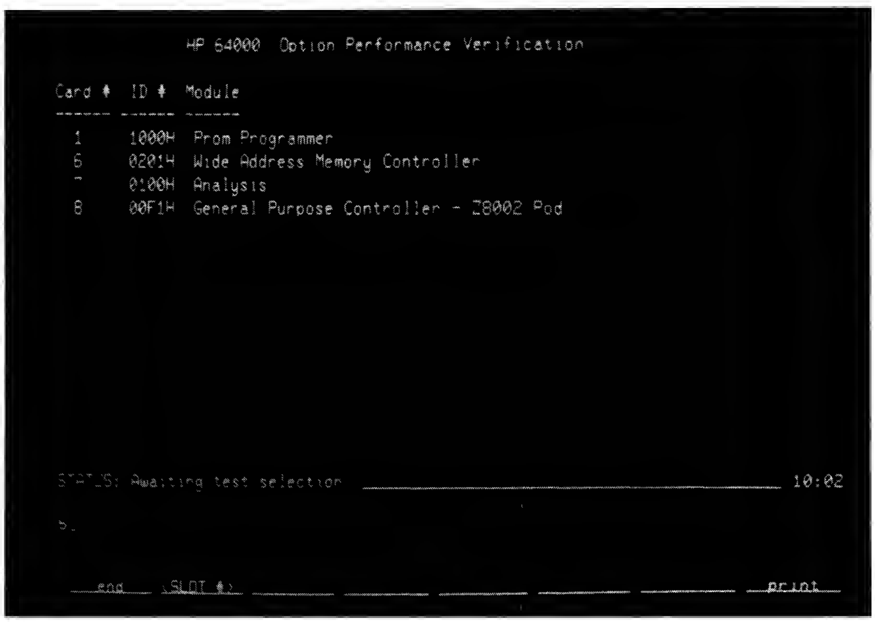


Figure 4-2. Slot Selection

4-9. The CRT will now show the overview display as shown in figure 4-3.

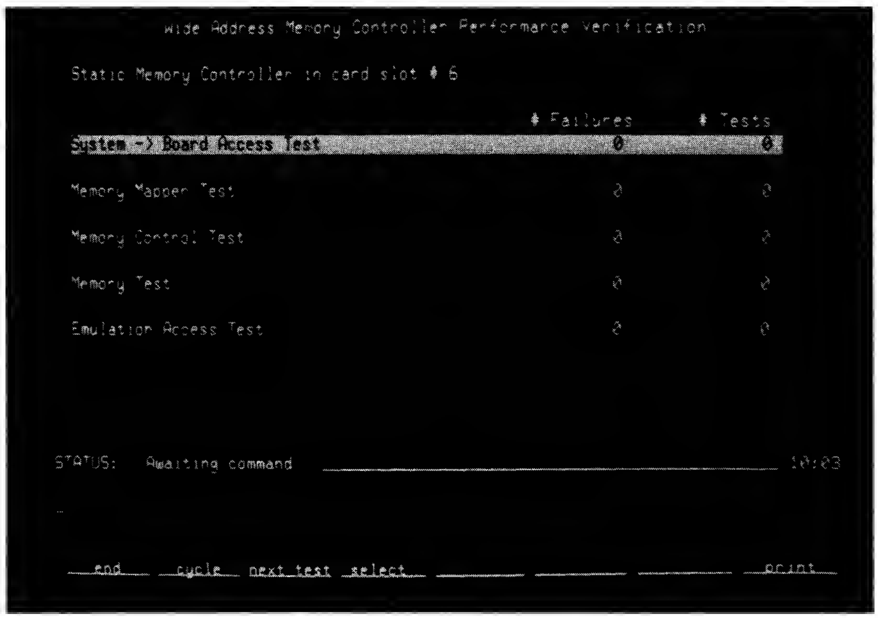


Figure 4-3. Overview Display

4-10. The Softkeys present in the overview display have the following functions:

end Halts execution of the Wide Address Memory Controller Tests.

cycle Continuously cycles through all of the tests noted in the overview display except for the Emulation Access Test which is skipped when cycling. Normally this would be the first key depressed to cycle through the tests and indicate any failures which can then be investigated more closely. However, a specific test can be specified without cycling at this level.

next_test Moves the inverse video bar to the next test to be run.

select Selects the test indicated by the inverse video bar for further investigation of failures. This key does not start the test but rather displays the failure information gathered from cycling at the overview level.

print Provides a hard copy of the current display above the STATUS line provided a printer is connected to the 64100. This key will work only if there are no tests in progress. If the printer is busy, the STATUS line will indicate "Waiting for Printer."

4-11. It is advisable at this time to press the cycle Softkey, run through several test cycles, and note if there are any failures. The inverse video bar will move from test to test as they are performed. After several test cycles have been run, press the end Softkey to stop cycling. If any test fails, the individual test can be run for a closer examination of the failure. This is explained in the following paragraphs.

4-12. Individual Test Selection Descriptions.

4-13. An individual test may be selected by pressing the next test softkey until the inverse video bar indicates the test to be investigated. The following Softkeys are present in the individual test displays.

SYSTEM -> BOARD ACCESS TEST SOFTKEYS

end	cycle	next_test	start				print

MEMORY MAPPER TEST SOFTKEYS

end	cycle	next_test	start				print

MEMORY CONTROL TEST SOFTKEYS

end	cycle	next_test	start				print

MEMORY TEST SOFTKEYS

end	cycle	next_test	start		img test	retn test	print

EMULATION ACCESS TEST SOFTKEYS

end	cycle	next_test	start			calib.	print

4-14. The Softkeys present in the individual displays have the following functions:

end	Returns to the overview level.
cycle	Cycles through all tests shown in the given test display.
next_test	Moves the inverse video bar to a specific test to be run.
start	Causes the test indicated by the inverse video bar to be run continuously at a high repetition rate. The high repetition rate is useful as it will provide a stable display on an oscilloscope. Also, when cycling the Memory Mapper and Emulation Access Test, the results will alternate if they are different for the two modes. Running only one test will provide a stable cumulative result.
print	Provides a hard copy of the current display above the STATUS line provided a printer is connected. This key will work only if no tests are in progress. If the printer is busy, the STATUS line will show "Waiting for Printer."
img test	See Memory Test Description.
retn test	See Memory Test Description.
calib.	See Emulation Access Test Description.

4-15. System -> Board Access Test Description.

4-16. The System -> Board Access Test can be run without working memory. When run, Interrupt and Access Status tests are performed at a very basic level. Interrupt Status checks to see if HROM and HGRD (U65-7,9) can be set and cleared individually. The Access Status Test checks to see if the Access Status Bit will set and clear properly when the CPU is attempting to make a successful access. Figure 4-4 shows a System -> Board Access Test Display and table 4-1 explains how to interpret test failures.

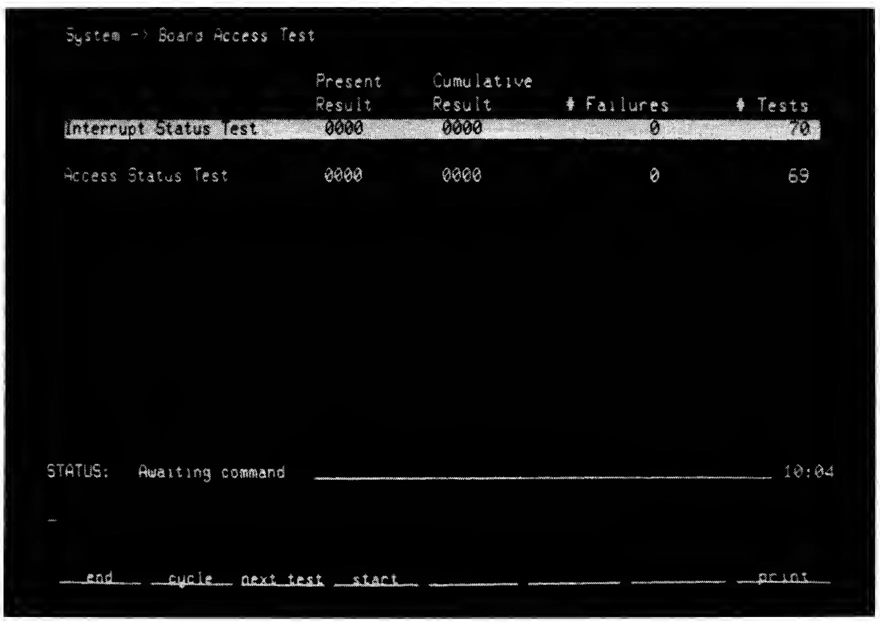


Figure 4-4. System -> Board Access Test Display

Table 4-1. System -> Board Access Test Results

Test	Result	Interpretation
Intr Status	0001	Can't set HROM
Intr Status	0010	Can't set HGRD
Intr Status	0011	Can't clear Status bits after setting them
Intr Status	1100	Can't clear the Interrupt Status Bits Initially
Acc Status	0001	Unable to set status bit to normally high
Acc Status	0010	Status bit did not go low to indicate lack of access
Acc Status	0011	Status bit did not go high to indicate successful access

4-17. Memory Mapper Test Description.

4-18. The Memory Mapper Test performs five tests on the addresss and data buses in two configurations and requires at least one row of good memory at address 0000H to provide valid results for the 64155A. The first test checks the data bus in the word mode. If any opens or supply shorts are detected, it prevents execution of the other tests. Next, it indicates which lines are failing and sets a flag to note that the remainder of the tests were not performed. If there are no supply shorts or opens, the data bus is next tested in the word mode for data lines shorted to each other. If this test fails, the remaining tests are aborted and a flag is set to note they were not performed. Any shorted lines are reported in both the word and byte mode results. If the data bus passes in the word mode, it is then tested in the byte mode to check for data lines shorted together and byte write strobes shorted together. In all cases, if the first three tests do not all pass, the STATUS line will display, for a short time, an error message noting that the software was unable to access memory location zero. If these three tests do pass, all remaining tests will be performed without aborts, regardless of their results.

4-19. The System Address Bus Test walks 1's and 0's across LA0 - LA10. This creates unique bit patterns which are read back to check the lines for being open or shorted together, or shorted to a power supply line.

4-20. The Mapper Image Test checks the Mapper RAM output for problems that would create images in memory. Since the amount of memory can be variable, this test checks to see how much memory is available and masks off failures which could not possibly exist due to the lack of memory present. This masking process is not impervious to failure. The fast access rates used by this board does not allow the charge stored on the data bus to bleed off and may allow erroneous results to appear in some instances. However, this is rare. Without a full complement of memory, there will rarely be any failures reported with walking 0's. The address lines checked by this test are A11 - A15. The System Address Register Test walks 1's and 0's across the upper address register to test for shorts and opens on the outputs of the register. If the Image Test indicates that A11 is failing, the register test will show "0FFF" on the results for both walking 1's and 0's. The Memory Mapper Test Display is shown in figure 4-5 and table 4-2 explains how to interpret test failures.

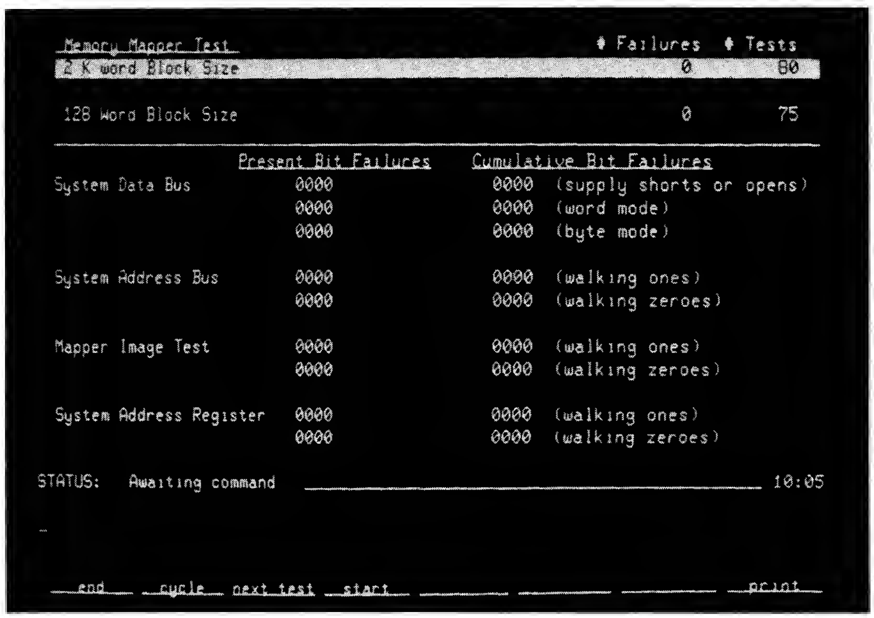


Figure 4-5. Memory Mapper Test Display

Table 4-2. Memory Mapper Test Results

Test	Result	Interpretation
Data Bus Test	xxxx	D15 - D0 in hex
Addr Bus Test 2k mode	_xxx	MA10 - MA0 in hex (right justified)
Addr Bus Test 128 mode	__xx	MA6 - MA0 in hex (right justified)
Mppr Img Test 2k mode	_xx_	MA15 - MA11 in hex (right justified in the x's)
Mppr Img Test 128 mode	_xxx	MA15 - MA7 in hex (right justified)
Addr Reg Test	_xxx	Address Register outputs MSB to LSB, left to right
All Tests Except Data Bus Tests	F000	Test was not performed due to data bus failure
Data Bus Test Byte Mode	FF00	If word mode showed no failures, this usually indicates that the memory write strobes are shorted together.
Addr Bus Test walking 1's	1xxx	This means that address 0000H failed also
Addr Bus Test walking 0's	1xxx	This means that address 0FFFH failed also

4-21. Memory Control Test Description.

4-22. There are four tests associated with the Memory Control Test. The Block Size Select Option test checks the ability to select between a 2k word block size and a 128 word block size.

4-23. The Real-time Access Test checks to see, when real time is NOT selected and the emulator is halted, that the CPU can access Emulation Memory. Also, it checks to see, when real time is selected and the emulator is halted, that the CPU can NOT access Emulation Memory. In the latter, transitions are not occurring on HMAV when the emulator is not running. These transitions are necessary to initiate an access to memory in the real time mode. Effectively therefore, this test checks the ability to program CNTLA (U96-11) to a 1 or 0.

4-24. The Allow Writes to ROM Option Test checks to see that interrupts will not occur (even though enabled by the CPU) when HROM (U65-9) is set and writes to ROM are allowed. This indirectly checks to see if a Break will occur since both LIR1 (U86-8) and LBRK (U54-12) are controlled by the same signal. The successful completion of the Memory Controller Interrupt Option Test will validate this indirect test. If this indirect test fails, the results of the Allow Writes to ROM Test may not be valid. That is, if the output of U86-8 (LIR1) is bad, the Allow Writes to ROM Test will never fail.

4-25. The Memory Controller Interrupt Option Test checks to see that an interrupt is generated (when enabled) if either HROM or HGRD (U65-7,9) is set. It also checks to see that those interrupts are cleared. The Memory Control Test Display is shown in figure 4-6.

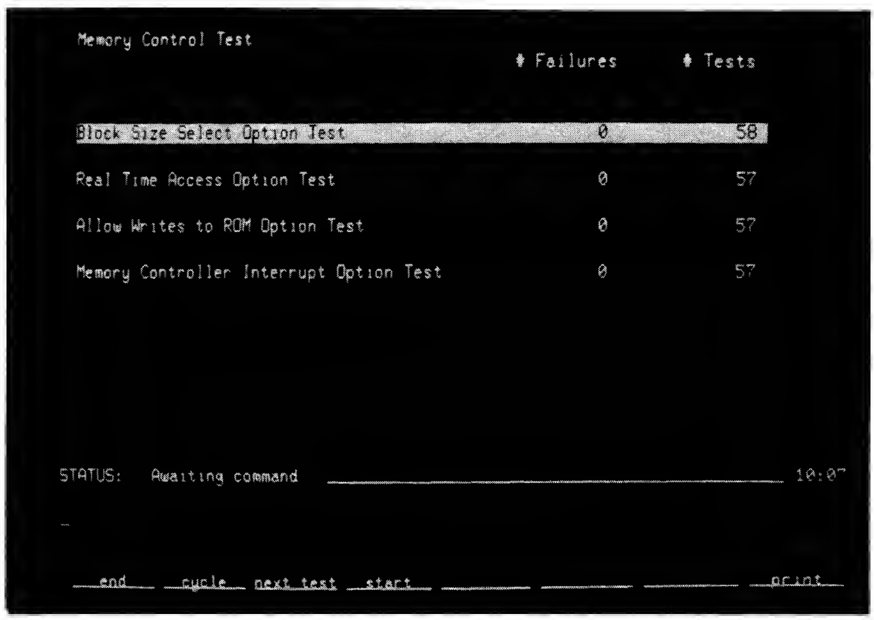


Figure 4-6. Memory Control Test Display

4-26. Memory Test Description.

4-27. The Memory Test checks the static RAM boards that the Memory Controller is connected to via the Memory Bus. Primarily, this test assumes a perfectly working Memory Controller Board and does not abort if there is a failure. However, if a known good Memory Board(s) is used, clues to problems on the Memory Controller Board can be obtained.

4-28. The Memory Test includes three types of tests. The first, and the only one activated by cycling, is the memory cell read/write test. This test writes and immediately reads back a random pattern in all cells in a selected row of memory. This is followed by reading back all of the block of memory to see if any cell was overwritten by an image. The data failure results are displayed in a cumulative form.

4-29. The next test is the Image Test and is activated by pressing the "img test" Softkey. This test was developed for use primarily in a production environment and checks for pins on the 6147 RAMs that do not make proper socket contact. However, it may be used for finding address line problems in blocks of memory above the first block, which is the only one tested in the Memory Mapper Test. The Memory Mapper Test does not test above the first block of addresses because only one row of RAM (corresponding to one memory block in this test) is required to be installed in the system. If a block of memory is chosen where no memory resides, the Image Test is rarely valid because of the data line charge problem discussed in paragraph 4-20.

4-30. The third test is the Retention Test and is activated by pressing the retn test Softkey. This test can only be aborted by a pressing the RESET key twice. This test takes about two minutes to run. When it is running, a countdown is displayed for both passes through memory. On the first pass, 0's are written to memory and read back approximately fifty seconds later. On the second pass, 1's are written to memory and read back approximately fifty seconds later. The test aborts upon finding a failure. Thus, depending on where the test stops, a 1 or 0 failure can be detected. The results of the Image and Retention Tests are displayed in the same area of the CRT, and they overwrite each other. If no failures are found, this will be noted on the STATUS line and the result area will be cleared. If there is a failure in any of the tests, the address it occurred at in a chosen block of memory is displayed in hex as well as the data bits that failed.

4-31. Neither the Image nor Retention Test will increment the test or fail counters because they are not a part of the normal test procedure. They are meant to be used for Image testing on a production checkout basis and as a last resort test for extremely rare occurrences of soft failures in static RAMs. The Memory Test Display is shown in figure 4-7.

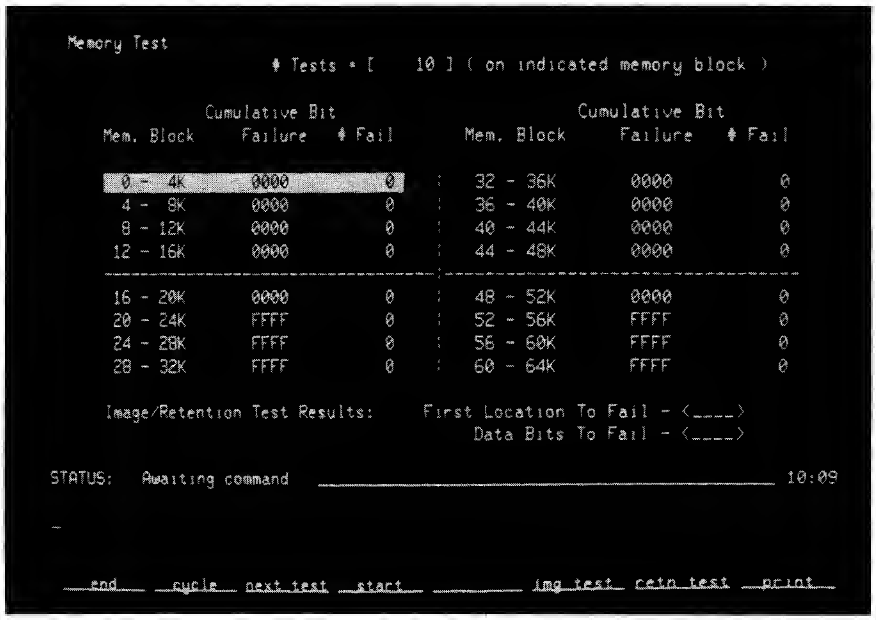


Figure 4-7. Memory Test Display

4-32. Emulation Access Test Description.

NOTE

Before running the Emulation Access Tests, disconnect the Emulation Bus Cables and leave only the Memory Bus Cable connected. In the Overview Display this test is skipped over when cycling. However, at this level, a continuous error message will be displayed if the start, cycle or calib Softkeys are pressed unless the Emulation Bus Cables are removed.

4-33. The Emulation Access Test performs six tests on the emulation access circuitry in two configurations and requires at least one row of good memory at address 0000H to provide valid results for the 64155A. The first test is on the data bus in the word mode. If any opens or supply shorts are found, the test aborts, preventing execution of any other tests. If the test aborts, the failures are displayed and a flag is set to note that the remainder of the tests were not performed. If there are no opens or supply shorts the data bus is next tested in the word mode for data lines shorted to each other. If this test does not pass, the lines that are shorted together are reported in both the word and byte mode results and a flag is set to note that the remaining tests were not performed. If the data bus passes in the word mode, it is then tested in the byte mode for data lines shorted together and byte write strobes shorted together. Unless all three tests pass, the STATUS line will display, for a short time, an error message indicating that the software was not able to access location zero. If they do pass, the address tests will be performed regardless of their results.

4-34. The Emulation Address Bus Test first checks the unmapped bits by walking 1's and 0's across LEA1 - LEA11. This creates a set of unique bit patterns which are read back to check for address line problems. The mapped bits are then tested by walking 1's and 0's across LEA23-LEA12 to test for problems on the inputs of the Mapper RAMs.

NOTE

If there is a problem with MA11 (A16), it will cause erroneous results for the Emulation Address Bus Test.

In the 128 word mode the 1's and 0's are walked across LEA1 - LEA7 and LEA19 - LEA8 respectively. If there are any failures in the mapped bits, the Timing and Status Tests are not run.

4-35. The Timing Test checks to see that writes to ROM and Guarded Memory cause the appropriate status bits to be set. It also checks to see that writes to User Memory do not cause a memory modification to occur or status bits to be set.

4-36. The calib Softkey is used to provide a stable scope display when setting the U66 one shot via the R27 potentiometer. This adjustment is critical (125 ns +-5 ns) and is explained in Section V. If the cables are attached, an error message will be displayed.

4-37. The Emulation Access Test Display is shown in figure 4-8. Table 4-3 explains how to interpret failures.

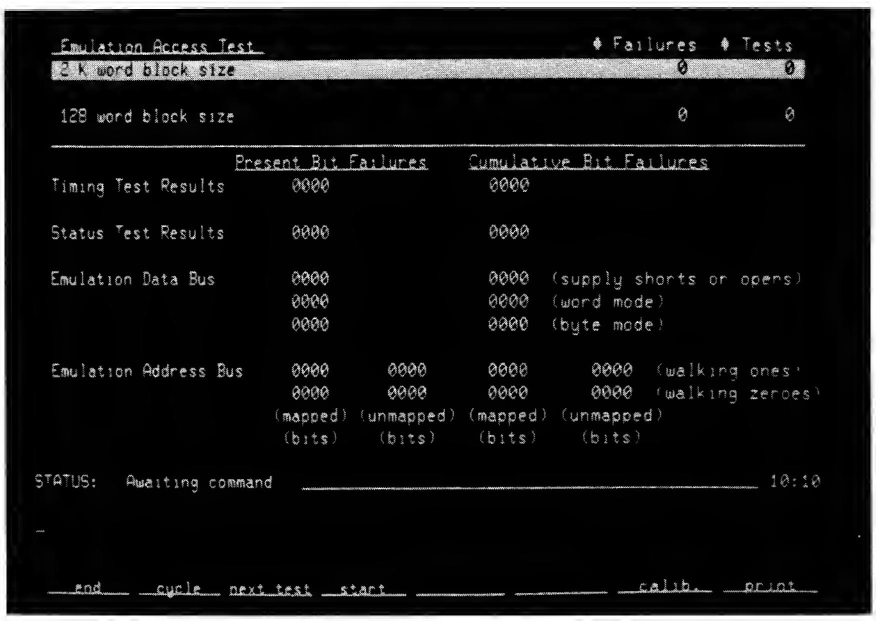


Figure 4-8. Emulation Access Test Display

Table 4-3. Emulation Access Test Results

Test	Result	Interpretation
Data Bus Test	xxxx	LED15 - LED0 in hex
Unmapped Bits 2k mode	_xxx	LEA7 - LEA1 in hex (right justified)
Unmapped Bits 128 mode	__xx	LEA7 - LEA1 in hex (right justified)
Mapped Bits 2k mode	_xxx	LEA23 - LEA12 in hex (right justified)
Mapped Bits 128 mode	_xxx	LEA19 - LEA8 in hex (right justified)
All Tests Except Data Bus Tests	F000	Test was not performed due to previous failure
Data Bus Test Byte Mode	FF00	If word mode showed no failures, this usually indicates that the memory write strobes are shorted together
Unmapped Bits walking 1's	1xxx	This means that address 000H failed also
Addr Bus Test walking 0's	1xxx	This means that address 0FFFH failed also
Timing Test	1100	Means that the configuration using the leading edge of WDAV and a 0 ns setup time of address input to HMAV going low, didn't work.
Timing Test	0001	Means that the configuration using the leading edge of WDAV and a 64 ns setup time of address input to HMAV going low, didn't work.

Table 4-3. Emulation Access Test Results (Cont'd)

Test	Result	Interpretation
Timing Test	0010	Means that the configuration using the trailing edge of WDAV and a 0 ns setup time of address input to HMAV going low, didn't work.
Status Test	0001	Write to ROM status bit did not set.
Status Test	0010	Write to GUARDED Memory status bit did not set.
Status Test	0011	Both status bits went high when only one should have.
Status Test	xFxx	Write to Emulation Memory was not prevented when a write to either USER, ROM or GUARDED Memory was performed.
Status Test	xExx	Read from Emulation Memory was not prevented when a read from USER Memory was performed.
Status Test	Fx01 Fx10 Fx11	ROM | Write to USER Memory GRD | set the indicated BOTH | status bits.

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. There is one adjustment on the 64155A Wide Address Memory Controller. This is the RDY STB adjustment which is used for the Emulation Access Test. RDY STB is adjusted at the factory and normally will not have to be changed. If it is changed, an oscilloscope should be used that is capable of measuring a pulse width of 125 ns (+ or -5 ns).

5-3. SAFETY CONSIDERATIONS.

5-4. There are no safety hazards associated with the 64155A Wide Address Memory Controller. There are, however, high voltages associated with the 64100 Mainframe. Appropriate warnings are given where a hazard may exist.

5-5. EQUIPMENT REQUIRED.

5-6. An oscilloscope capable of measuring a negative going pulse width of 125 ns (+-5 ns).

5-7. RDY STB ADJUSTMENT.

5-8. Use the following procedure to adjust RDY STB.

a. Turn the 64100 Mainframe power switch to the OFF position and remove all Bus Cables.

b. Place the 64155A Wide Address Memory Controller on an extender board.

c. Reconnect the Memory Bus Cable. Do NOT reconnect the Emulation Bus Cables.

d. Turn the 64100 Mainframe power switch to the ON position.

e. Refer back to the performance verification in Section IV and select the Emulation Access Test.

f. With the Emulation Access Test Display on the CRT, press the calib Softkey.

g. Refer to figure 5-1 and connect the oscilloscope probe to the RDY STB test point. A Convenient GND is located just below the RDY STB test point. This GND should be used for grounding the oscilloscope probe (the use of a spanner tip probe is recommended).

h. Adjust R27 (see figure 5-1) for a 125 ns negative going pulse width as shown in figure 5-2. This adjustment must be within + or -5 ns.

i. Turn the 64100 Mainframe power switch to the OFF position and reinstall the 64155 Wide Address Memory Controller in the cardcage.

j. Reconnect the Memory and Emulation Bus Cables.

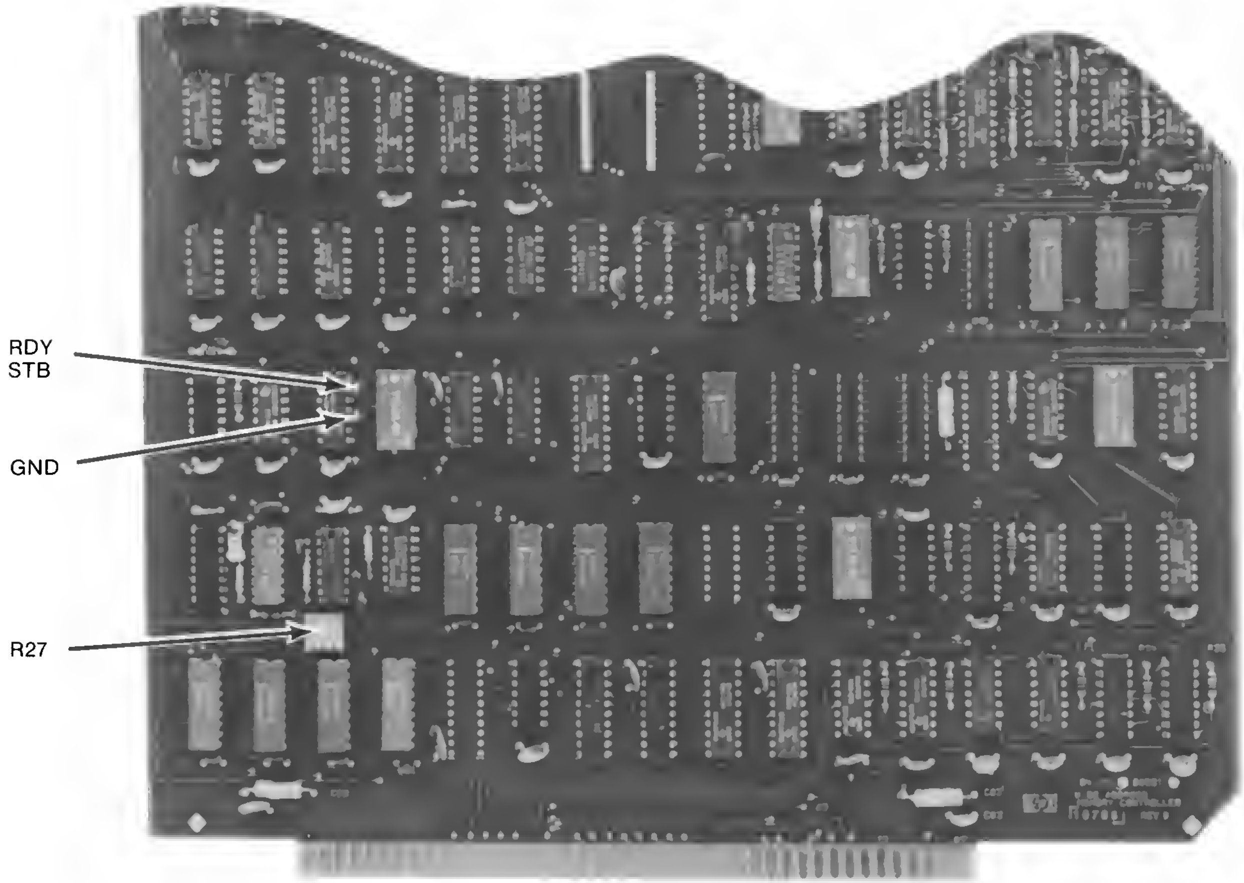


Figure 5-1. Emulation Access Timing Adjustment Test Points

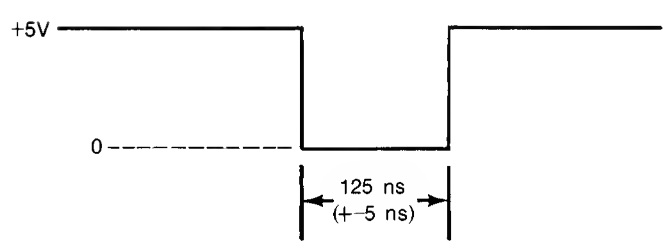


Figure 5-2. RDY STB Pulse Width

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information concerning replaceable parts. Table 6-1 lists abbreviations used in the parts list and throughout this manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five digit numbers.

6-3. EXCHANGE ASSEMBLIES.

6-4. The Model 64155A is a part of the Hewlett-Packard Corporation's Blue Stripe Exchange program. New assemblies required for spare parts stock must be ordered by the new assembly part number listed in table 6-2. Factory repaired and tested assemblies are available on a trade in basis only by ordering the following rebuilt part number:

64155-69501

6-5. ABBREVIATIONS.

6-6. Table 6-1 lists abbreviations used in the parts list, on the schematics and throughout this manual. In some cases, two forms of the abbreviations are used: one all in capital letters and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, on the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-7. REPLACEABLE PARTS.

6-8. Table 6-2 is the list of replaceable parts and is organized by components in alphanumerical order by reference designator.

6-9. The information for each part consists of the following:

a. The Hewlett-Packard part number and the check digit.

b. The total quantity (Qty) used on the PC board.

c. The description of the part.

d. A five digit code that indicates the manufacturer.

e. The manufacturer's part number.

6-10. The total quantity for each part is given at the first appearance of the part number on the list.

6-11. For ordering information, see Section VI of the 64100 Mainframe Tab.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		bulb, photocell, etc
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64155-66501	0	1	WIDE ADDRESS MEMORY CONTROLLER BOARD	28480	64155-66501
C1	0160-3622	8	22	CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C2	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C3	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C4	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C5	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C6	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C7	0160-2055	9	53	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	20480	0160-2055
C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	20480	0160-2055
C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C30	0140-0190	7	1	CAPACITOR-FXD 39PF +-5% 300VDC MICA	72136	DM15E390J0300WV1CR
C31	0180-0373	2	1	CAPACITOR-FXD .68UF+-10% 35VDC TA	56289	150D684X9035A2
C32	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C33	0160-3622	0		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C34	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C35	0160-3622	0		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C36	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C37	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C38	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C39	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C40	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C41	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C42	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C43	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C44	0160-3622	0		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C45	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C46	0180-0229	7	3	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C47	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C48	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C49	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C50	0160-2235	7	1	CAPACITOR-FXD .75PF +-.25PF 500VDC CER	28480	0160-2235
C51	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C52	0160-4492	2	1	CAPACITOR-FXD 18PF +-5% 200VDC CER 0+-30	51642	200-200-NP0-180J
C53	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C54	0140-0194	1	1	CAPACITOR-FXD 110PF +-5% 300VDC MICA	72136	DM15F111J0300WV1CR
C55	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C56	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C57	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C58	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C59	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C60	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C61	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C62	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C63	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C64	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C65	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C66	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C67	0160-3622	0		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C68	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z
C69	0160-3622	8		CAPACITOR-FXD .1UF +80-20% 100VDC CER	26654	2130Y5V100R104Z

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
C70	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C71	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C72	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C73	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C74	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C75	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C76	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C77	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C78	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C79	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C80	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C81	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C82	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C83	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
R1	0757-0442	9	19	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R3	0698-3383	7	13	RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R4	0698-3383	7		RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R5	0698-3383	7		RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R6	0698-3383	7		RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R7	0698-3383	7		RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R8	0698-3383	7		RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R9	0698-3383	7		RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R10	0698-3383	7		RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R11	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R12	0698-3383	7		RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R13	0698-3383	7		RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R14	0698-3383	7		RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R15	0698-3383	7		RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R16	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R17	0757-0438	3	5	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R18	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R19	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R20	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R21	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R23	0698-3383	7		RESISTOR 56 1% .125W F TC=0+-50	24546	NC4-1/8-T2-56R0-F
R24	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R25	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R26	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R27	2100-3252	6	1	RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN	28480	2100-3252
R28	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R29	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R30	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R31	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R32	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R33	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R34	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R35	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R36	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R37	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R38	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
U1	1820-1633	8	2	IC BFR TTL S LINE DRVR OCTL	01295	SN74S240N
U2	1820-1633	8		IC BFR TTL S LINE DRVR OCTL	01295	SN74S240N
U3	1820-2699	8	4	IC-74F241	28480	1820-2699
U4	1820-2699	8		IC-74F241	28480	1820-2699
U5	1820-2699	8		IC-74F241	28480	1820-2699
U6	1820-2699	8		IC-74F241	28480	1820-2699
U7	1820-2075	4	4	IC MISC TTL LS	01295	SN74LS245N
U8	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U9	1820-1428	9	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
U10	1820-1428	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
U11	1820-1439	2	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
U12	1820-2024	3	8	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U13	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U14	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U15	1820-1158	2	2	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U16	1820-1158	2		IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U17	1820-2684	1	4	IC-74F00	28480	1820-2684
U18	1820-2685	2	5	IC-74F02	28480	1820-2685
U19	1820-1997	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U20	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U21	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U22	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U23	1810-0280	8	2	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
U24	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
U25				NOT ASSIGNED		
U26	1810-0555	0	3	DELAY LINE-50NS	28480	1810-0555
U27	1820-2685	2		IC-74F02	28480	1820-2685
U28	1820-2695	4	3	IC-74F158	28480	1820-2695
U29	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U30	1820-2695	4		IC-74F158	28480	1820-2695
U31	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U32	1820-2695	4		IC-74F158	28480	1820-2695
U33	1820-1275	4	3	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U34	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U35	1820-2685	2		IC-74F02	28480	1820-2685
U36	1820-2506	6	4	IC INV TTL F HEX	07263	74F04PC
U37	1820-2687	4	1	IC-74F10	28480	1820-2687
U38	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U39	1820-1198	0	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
U40				NOT ASSIGNED		
U41	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U42	1820-1782	8	2	IC MV TTL S MONOSTBL RETRIG/RESET DUAL	34335	AM26S02PC
U43	1810-0555	0		DELAY LINE 50NS	28480	1810-0555
U44	1820-2691	0	2	IC-74F74	28480	1820-2691
U45				NOT LOADED		
U46	1818-1586	5	12	IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	34649	D2147H-1
U47	1818-1586	5		IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	34649	D2147H-1
U48	1818-1586	5		IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	34649	D2147H-1
U49	1820-2691	0		IC-74F74	28480	1820-2691
U50	1820-2684	1		IC-74F00	28480	1820-2684
U51	1820-2685	2		IC-74F02	28480	1820-2685
U52	1810-0556	1	1	DELAY LINE-60NS	28480	1810-0556
U53	1820-2686	3	3	IC-74F08	28480	1820-2686
U54	1820-0684	7	1	IC INV TTL S HEX 1-INP	01295	SN74S05N
U55	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U56	1820-2506	6		IC INV TTL F HEX	07263	74F04PC
U57	1818-1586	5		IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	34649	D2147H-1
U58 - U60	NOT LOADED			NOT ASSIGNED		
U61						
U62	1820-2684	1		IC-74F00	28480	1820-2684
U63	1810-0554	9	1	DELAY LINE-40NS	28480	1810-0554
U64	1820-2684	1		IC-74F00	28480	1820-2684
U65	1820-2693	2	1	IC-74F109	28480	1820-2693
U66	1820-1782	8		IC MV TTL S MONOSTBL RETRIG/RESET DUAL	34335	AM26S02PC
U67	1820-1423	4	1	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
U68	1820-2690	9	1	IC-74F32	28480	1820-2690
U69	1818-1586	5		IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	34649	D2147H-1
U70	1818-1586	5		IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	34649	D2147H-1
U71	1818-1586	5		IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	34649	D2147H-1
U72	1818-1586	5		IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	34649	D2147H-1
U73				NOT ASSIGNED		
U74	1820-2506	6		IC INV TTL F HEX	07263	74F04PC
U75	1810-0555	0		DELAY LINE-50NS	28480	1810-0555
U76	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U77	1820-0629		3	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112
U78	1820-2686	3		IC-74F08	28480	1820-2686
U79	1820-2506	6		IC INV TTL F HEX	07263	74F04PC
U80	1820-2685	2		IC-74F02	28480	1820-2685
U81	1818-1586	5		IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	34649	D2147H-1
U82	1818-1586	5		IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	34649	D2147H-1
U83	1818-1586	5		IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	34649	D2147H-1
U84	1818-1586	5		IC NMOS 4096 (4K) RAM STAT 35-NS 3-S	34649	D2147H-1
U85				NOT ASSIGNED		
U86	1820-0682	5	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S03N
U87	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U88	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U89	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U90	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U91	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U92	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U93	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U94	1820-2686	3		IC-74F08	28480	1820-2686
U95	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112
U96	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112
W1	64151-61602	8	1	MEMORY BUS CABLE FOR J1 (2 CONN)	28480	64151-61602
W2	64151-61603	9	1	MEMORY BUS CABLE FOR J1 (3 CONN)	28480	64151-61603
W3	64151-61604	0	1	MEMORY BUS CABLE FOR J1 (4 CONN)	28480	64151-61604
	64151-61605	1	1	MEMORY BUS CABLE FOR J1 (5 CONN)	28480	64151-61605

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
XU42	1200-0607	0	3	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU46	1200-0539	7	12	SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU47	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU48	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU54	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
XU57	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU66	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU67	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU69	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU70	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU71	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU72	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU81	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU82	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU83	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU84	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
	64155-90901	5	1	SERVICE MANUAL	28480	64155-90901

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
26654	VARADYNE INC	SANTA MONICA	CA	90404
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
51642	CENTRE ENGINEERING INC	STATE COLLEGE	PA	16801
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC	CT	06226

See introduction to this section for ordering information

SECTION VII

MANUAL CHANGES

7-1. This section normally contains information for backdating this manual for models with a repair number prefix prior to the one shown on the title page. Because this edition includes the information for the first repair number prefix assigned, no backdating is required.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains block diagrams, schematics and theory of operation for the 64155A Wide Address Memory Controller.

8-3. Emulation System Block Diagram Description.

8-4. Figure 8-1 is a basic block diagram of an emulation system and shows the placement of the 64155A Wide Address Memory Controller in the system.

8-5. The 64155A Wide Address Memory Controller is the interface between Emulation Memory, the installed Emulator, and the 64000 operating system. This option also maps the users address received via the Emulation Bus into available Emulation Memory. The mapping process is performed by Mapper RAMs which reside on the Memory Controller. In a 16 bit emulation system, up to four Low Power Emulation Memory Boards (HP Model 64152B, 64153B or 64154B) can be installed. A read/write operation to Emulation Memory is performed via the Memory Bus.

8-6. The Mapper RAMs also output signals which specify what type of memory the given block of Emulation Memory is supposed to act like (RAM, ROM or GUARDED Memory), or whether a given address is to be regarded as user address space and not acted upon. The Memory Controller will also signal the analysis equipment and halt emulation when a GUARDED memory access is attempted and, if optionally configured, when a write to ROM is attempted.

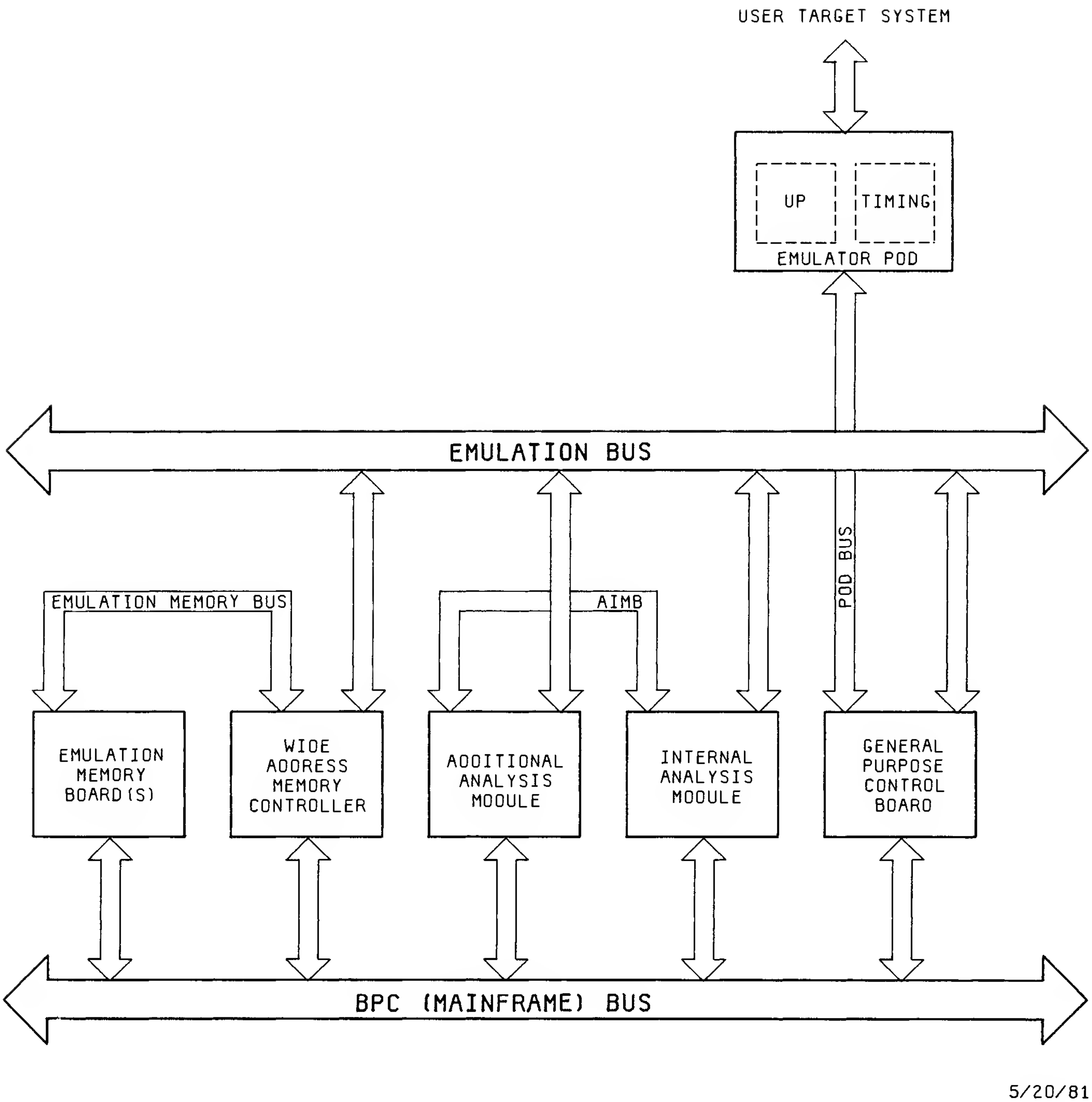


Figure 8-1. Emulation System Block Diagram

8-7. 64155A Wide Address Memory Controller Block Diagram.

8-8. A detailed block diagram of the 64155A Wide Address Memory Controller is shown six times in this section. Each time it is repeated, the shaded area will represent the circuitry for an associated schematic. A circuit description, which includes this block diagram level, is given after the mnemonic table.

8-9. Signal Mnemonics.

8-10. Table 8-1 lists the signal mnemonics used on the schematics and in the theory of operation in this section:

Table 8-1. Signal Mnemonics

Mnemonic	Meaning	Origin
25 MHz	25 MHz system clock.	CPU Bus, Schematic 1.
B25 MHz	Buffered 25 MHz. Buffered version of the 25 MHz system clock.	U79-12, Schematic 1.
CNTLA	Control "A". Control signal that determines whether or not the CPU waits for the emulator to finish a memory access before it begins its own access.	U55-19, Schematic 5.
CNTLB	Control "B". Control signal that determines whether or not emulation address must be set up for 64 ns before the falling edge of HMAV.	U55-16, Schematic 5.
CNTLC	Control "C". Control signal that determines which edge of LWDV is used to strobe write data into Emulation Memory.	U55-15, Schematic 5.
CNTLW	Control Write. Signal that clocks the control bits into the control register.	U91-13, Schematic 4.
CPUWSTB	CPU Write Strobe. Initiates a write for the CPU.	U62-11, Schematic 2.
DRVEM	Drive Emulator Bus. When low this signal enables the data bus buffers to drive the emulation bus for a read operation from Emulation Memory.	U50-11, Schematic 3.

Table 8-1. Signal Mnemonics (Cont'd)

Mnemonic	Meaning	Origin
EMWSTB	Emulation Write Strobe. Write strobe for the write strobe generation circuitry. Generated by the emulation access circuitry.	U18-4, Schematic 2.
HBSTM	High Buffered Start Memory. Inverted, buffered version of LSTM. Gated via U62B to enable the U42B one shot to start a CPU memory access timeout.	U74-4, Schematic 4.
HCOMPL	High Complete Access. Status bit which is high if the CPU assess to Emulation Memory just performed was completed successfully.	U44-9, Schematic 1.
HDISCONB	High Disconnected Cable B. High if cable "B" is disconnected. This is the center Emulation Bus Cable.	Emulation Bus, Schematic 5.
HDISCONC	High Disconnected Cable "C". High if cable "C" is disconnected. This is the Emulation Bus cable located on the upper right side of the board, as viewed from the front of the mainframe.	Emulation Bus, Schematic 5.
HGRD	High Guarded. Status bit which is high if an access to guarded memory was made.	U65-7, Schematic 3.
HMAV	High Memory Available. When high, the emulator is not presently making an access to Emulation Memory.	Emulation Bus, Schematic 3.
HREAD	High Read. High when a read from Emulation Memory is being performed. This signal enables the Data Bus Drivers on the Memory Board.	U17-11, Schematic 2.
HREADY	High Ready. When this signal goes high an Emulator Memory access has been completed.	U68-11, Schematic 3.
HROM	High ROM. Status bit which is high to note an access to ROM was made.	U65-9, Schematic 3.
HWDV	High Write Data Valid. The inverted version of LWDV which is gated to generate the Emulation Write Strobe (EMWSTB).	U56-12, Schematic 3.

Table 8-1. Signal Mnemonics (Cont'd)

Mnemonic	Meaning	Origin
LA0-LA10	Low Address 0-10. 64000 System address lines, active low.	CPU Bus, Schematic 4.
LA12, LA13	Low Address 12, 13. 64000 System address lines, active low.	CPU Bus, Schematic 4.
LBA0-LBA10	Low Buffered Address 0-10. Buffered system address lines.	U89, U90, Schematic 4.
LBBPOP	Low Buffered Buffered Power On Preset. LPOP which has been buffered twice for fan out reasons.	U94-8, Schematic 2.
LBBYTE	Low Buffered Byte. Buffered version of LBYTE.	U89-12, Schematic 2.
LBPOP	Low Buffered Power On Preset. LPOP which has been buffered once.	U94-6, Schematic 2.
LBRK	Low Break. Pulls emulation break line which sends the Emulator into the Monitor Mode.	U54-12, Schematic 3.
LBSEL	Low Buffered Select. Buffered version of LSEL.	U89-9, Schematic 4.
LBSTB	Low Buffered Strobe. Buffered version of LSTB.	U89-7, Schematic 4.
LBSTM	Low Buffered Start Memory. Buffered version of LSTM.	U89-5, Schematic 4.
LBUPB	Low Buffered Upper Byte. Buffered version of LUPB.	U37-6, Schematic 2.
LBWRT	Low Buffered Write. Buffered version of LWRT.	U94-3, Schematic 4.
LBYTE	Low Byte. When low, indicates that a memory cycle is to involve an eight bit byte, rather than the full sixteen bits of the word.	CPU Bus, Schematic 2.
LCLSTA	Low Clear Status. Clears the HROM and HGRD status bits.	U78-6, Schematic 5.

Table 8-1. Signal Mnemonics (Cont'd)

Mnemonic	Meaning	Origin
LD0-LD15	Low Data 0 - 15. A 16 bit bi-directional bus used to transfer data to and from the CPU. When LSTB is low, data is present on the bus.	CPU Bus, Schematic 4.
LDISCON	Low Disconnected Cables. Signal which is low if both Emulation cables are disconnected.	U38-11, Schematic 5.
LEA1-LEA23	Low Emulation Address 1 - 23. Emulation address bus signals.	U12 - U14, Schematic 5.
LEBUP	Low Emulation Byte Upper. Same as LUPB except it comes from the Emulator instead of the CPU.	U41-12, Schematic 3.
LEBYT	Low Emulation Byte. Same as LBYTE except comes from Emulator instead of the CPU.	U41-9, Schematic 3.
LED0-LED15	Low Emulation Data 0 - 15. Emulation Data Bus lines.	U3 - U6, Schematic 7.
LGRD	Low Guard. Signal which goes low if the current Emulation Memory Access is mapped as Guarded Memory.	U2-14, Schematic 7.
LIDEN	Low Identification Enable. When low, enables all PC Boards in slots 0 thru 9 (option slots) to generate card-type ID codes after interrogation by the slot select command.	CPU Bus, Schematic 5.
LIDENG	Low Identify Enable Gated. This signal is used with LIDEN to enable the board ID code. This signal is generated by U92 via LBSTB and LBSEL.	U92-7, Schematic 4.
LIR1	Low Interrupt Request 1. Requests a system interrupt.	U86-8, Schematic 3.
LLA11 - LLA22	Low Latched Address 11 - 22. Outputs of the upper address register.	U29, U31, Schematic 5.
LLA19I - LLA22I	Low Latched Address 19 - 22 Inverted. The inverted version of the upper four bits of the upper address register.	U31, Schematic 5.

Table 8-1. Signal Mnemonics (Cont'd)

Mnemonic	Meaning	Origin
LMAP1 - LMAP3	Low Address Map 1 - 3. Extends address selection capability to 64k locations on each option card. Active low.	CPU Bus, Schematics 1, 2 and 4.
LMAP1G	Low Map 1 Gated. A version of LMAP1 which is used to enable the U19 and U21 readback latches.	U92-9, Schematic 4.
LMAP2G	Low Map 2 Gated. A version of LMAP2 which is used to enable U91.	U92-10, Schematic 4.
LMAP3G	Low Map 3 Gated. A version of LMAP3 which is gated with LBWRT to initiate the Mapper RAM write signal (LMPRWE).	U92-12, Schematic 4.
LMAV	Low Memory Available. Inverted version of HMAV which clocks U96.	U56-10, Schematic 3.
LMBRKS	Low Memory Break Status. This signal, when low, means that the memory controller pulled LBRK low and not the Analysis unit.	U56-2, Schematic 3.
LMD0-LMD15	Low Memory Data 0 - 15. Emulation Memory Data Bus.	Memory Bus/ U20, U22, Schematic 7.
LMPRWE	Low Mapper Write Enable. This is the write Strobe for the Mapper RAMs.	U62-3, Schematic 4.
LMSKINT	Low Mask Interrupts. When low this signal prevents the CPU from being interrupted when the memory controller pulls LBRK.	U55-9, Schematic 5.
LMSYN	Low Memory Sync. A signal from addressed devices. When low, forces the CPU to wait until the addressed devices can complete the read or write operation.	U54-4, Schematic 1.
LPOP	Low Power on Pulse. When low, initializes and prevents the CPU from running. When LPOP is released, the CPU begins operation at address 20 Hex.	CPU Bus, Schematic 2.

Table 8-1. Signal Mnemonics (Cont'd)

Mnemonic	Meaning	Origin
LPVEN	Low Performance Verification Enable. When this control bit is low the PV buffers and transceivers are enabled if the Emulation Bus cables have been removed.	U55-5, Schematic 5.
LPVENG	Low Performance Verification Enable Gated. This signal is generated by gating LPVEN and LDISCON. If PV is enabled and the Emulation Bus cables are disconnected, the PV buffers will be enabled.	U32-8, Schematic 5.
LPVRD	Low PV Read. This signal goes low when a PV read is being performed.	U91-10, Schematic 4.
LPVWRT	Low PV Write. This signal goes low when a PV write is being performed.	U91-11, Schematic 4.
LRDINT	Lcw Read Interrupt. This signal enables the interrupt status bits for a BPC read operation.	U91-12, Schematic 4.
LRDSTA	Low Read Status. This signal enables the HCOMPL and LDISCON status bits for a BPC read operation.	U91-14, Schematic 4.
LROM	Low ROM. This signal goes low when the current emulation access is from memory which is mapped as ROM.	U2-18, Schematic 7.
LROMEN	Low ROM Enable. When this control bit is low it allows a write to ROM to cause LBRK to be pulled.	U55-6, Schematic 5.
LSEL	Low Select. Slot select signal for the card cage.	CPU Bus, Schematic 4.
LSTB	Low Strobe. When low, and in the write mode, indicates the data bus has valid information on it. When low, and in the read mode, indicates the CPU is not driving the bus, and the device addressed can now drive it.	CPU Bus, Schematic 4.

Table 8-1. Signal Mnemonics (Cont'd)

Mnemonic	Meaning	Origin
LSTM	Low Start Memory. Used to initiate a memory cycle. When low, indicates the the information on the Address Bus is valid.	CPU Bus, Schematic 4.
LUPB	Low Upper Byte. When low, indicates the upper byte is being written or read and is used only when LBYTE is low.	CPU Bus, Schematic 4.
LUSER	Low User. When low this signal means that the current access being made by the emulator is from user memory.	U2-16, Schematic 7.
LUSERL	Low User Latched. Latched version of LUSER.	U49-5, Schematic 3.
LWADRUP	Low Write Address Upper. Write strobe for the upper address register.	U91-15, Schematic 4.
LWDV	Low Write Data Valid. A signal which is inverted and gated to generate the Emulator Write Strobe (EMWSTB).	U41-14, Schematic 3.
LWRL	Low Write Lower. Write strobe for the lower 8 bits of Emulation Memory.	U18-13, Schematic 3.
LWRT	Low Write. Read/Write status line for the CPU.	CPU Bus, Schematic 4.
LWRU	Low Write Upper. Write strobe for the upper 8 bits of Emulation Memory.	U18-1, Schematic 2.
MA0-MA19	Memory Address 0 - 19. Emulation Memory Address Bus.	U9 - U11 on Schematic 5 and U1, U2 on Schematic 7.
MD00-MD07	Mapper Data Out 0 - 7.	U81 - U84 and U69 - U72, Schematic 6.
MD08-MD015	Mapper Data Out 8 - 15.	U57 - U60 and U45 - U48, Schematic 6.
MPX	Multiplex. When high this signal turns the address multiplexer to point toward the CPU instead of the Emulator.	U74-10, Schematic 2.

Table 8-1. Signal Mnemonics (Cont'd)

Mnemonic	Meaning	Origin
$\overline{\text{MPX}}$	MPX Inverted. Inverted version of MPX used on the multiplexer which requires a low to turn toward the CPU.	U93-6, Schematic 2.
MRA0-MRA11	Mapper RAM Address 0 - 11. Address inputs to the Mapper RAMs.	U28, U30, U32, Schematic 5.
RCVEM	Receive Emulation Bus. When high this signal enables the Emulation Data Bus Transceivers so that data can be input from the Emulator during an emulation write operation.	U18-10, Schematic 3.
S	Select. This control bit selects the block size. When low the block size is 128 words, when high the block size is 2k words.	U55-12, Schematic 3.
$\overline{\text{S}}$	Select Inverted. Inverted version of select.	U56-6, Schematic 5.
SSMA	Sync Start Memory Access.	U64-11, Schematic 1.
STHGRD	Set HGRD. This signal goes low to set the HGRD status bit for Performance Verification.	U91-9, Schematic 4.
STHROM	Set HROM. This signal goes low to set the HROM status bit for Performance Verification.	U91-7, Schematic 4.

8-11. THEORY OF OPERATION.

8-12. Mapper RAMs.

8-13. The Mapper RAMs map the users address into available Emulation Memory. That is, a given address input is received from the Emulation Bus and is loaded into the RAMs. The data outputs of the RAMs then serve as the address for Emulation Memory. Three of the RAMs (U46, U47 and U48) are not used for generating a memory address. These three RAMs identify what type of memory the given block of Emulation Memory is supposed to act like. It can act like RAM, ROM or GUARDED memory, or a given address can be regarded as user address space and not acted upon. The resistors in series on the Mapper RAM address lines reduce ringing which might occur because of the high input impedance of the RAMs.

8-14. Data Buses.

8-15. There are essentially three data buses on this board:

CPU Data Bus (LD0-LD15)
Emulation Data Bus (LED0-LED15)
Memory Data Bus (LMD0-LMD15)

8-16. The CPU Data Bus is buffered immediately when it comes on board by the U87 and U88 transceivers. These transceivers are always enabled and normally point toward the Memory Controller. They point toward the CPU Bus when U37 pin 8 goes low. This only occurs when the board is selected (U36 pin 8 goes high), a read operation is being performed (LBWRT is high), and LSTB is active (U74 pin 6 is high).

8-17. After the incoming CPU Data Bus is buffered, it is routed to the Upper Address Register (U29 and U31), the Control Register (U55), the Memory Bus Write Buffers (U20 and U23), the Emulation Bus Transceivers (U7 and U8) and the Mapper RAM data inputs. Most read and write signals for the various registers and Mapper RAMs are generated by address decoders U92 and U93. The write strobe for the Mapper RAMs, however, is generated by U62 pin 3. This occurs each time U76 pin 10 goes positive. The duration of the write strobe is determined by the U75 delay line.

8-18. The Memory Bus Write Buffers are used to transfer write data from the CPU Bus to the Memory Bus during a CPU write to Emulation Memory. The CPU Readback Latches (U19 and U21) are used to latch data during a high speed memory read. This permits the CPU to read the latched data when it is ready thereby not tying it up for a microsecond or more at a time.

8-19. The Emulation Bus PV Transceivers connect between the Emulation Data Bus and the CPU Data Transceivers. They permit the CPU to look like an emulator during Emulation Bus Performance Verification cycles.

8-20. The Emulation Data Bus also connects to the PV Data Bus Transceivers. These permit the emulator to access Emulation Memory when necessary and are otherwise tri-stated.

8-21. The Emulation Memory Bus permits Emulation Memory to be accessed by both the CPU and read/write devices on the Emulation Bus.

8-22. Address Buses.

8-23. There are four address buses on this board:

The CPU Address Bus (LA0 - LA10)
Mapper RAM Address Bus (MRA0 - MRA11)
Memory Mapper Address Bus (MA0 - MA19)
Emulation Address Bus (LEA1 - LEA23)

8-24. The CPU Address Bus is buffered immediately upon entering the board by U89 and U90. After it is buffered, it connects to the Emulation Address Bus PV Buffers (U12 - U14) and the Memory/Mapper Address Bus Multiplexers (U9 - U11, U28, U30, U32). Also, the outputs of the Upper Address Register (U29 and U31) are a part of the CPU Address Bus. These latched outputs (LLA11 - LLA18) constitute the upper half of the CPU Address. The Emulation Address Bus PV Buffers, as previously noted, make the CPU look like an emulator during Emulation Bus PV cycles. The multiplexers select the proper address bus to drive the memory/mapper address lines. The inverted outputs of U31 duplicate the inversion caused by the discrete multiplexer on the Emulation Address Bus's upper 4 bits.

8-25. The Emulation Address Bus is connected to the Emulation Address PV Buffers and the Multiplexers. U15 and U16 form a discrete multiplexer which selects between LEA20 - LEA23 and LEA8 - LEA11 to go to the uppermost Mapper Address Bus Multiplexer. This in turn selects the block size the emulator will use.

8-26. The Memory Address Bus is normally formed by the outputs of U9 - U11. However, when the 128 word block size is selected, the outputs of U11 are tri-stated and the outputs of U1 pins 3, 5, 7 and 9 are enabled instead. The Mapper Address Bus is then formed by the data outputs of the Mapper RAMs as well as U9 and U10. The Mapper RAM outputs are buffered by U1 and U2 to provide the necessary drive for the Memory Board Address Buffers.

8-27. The Mapper RAM Address Bus is formed by the outputs of the U28, U30 and U32 Multiplexers. This bus provides the address for the Mapper RAMs.

8-28. Performance Verification Circuitry.

8-29. In addition to the circuitry already mentioned, U41, U53 pin 8, U38 pin 11, and U32 pin 8 test the Emulation Bus. U38 pins 12 and 13 determine if the Emulation Bus Cables have been removed. If not, grounds on the Emulation Bus will pull down these inputs which are pulled high by R1 and R16 when the cables are removed. If the cables are not removed, a status bit will flag the CPU of this. The PV buffers cannot be enabled unless the Emulation Bus Cables are removed. When LPVEN is set in the Control Register (U55), accesses through address 5XXX Hex with LMAP2 low will be directed through the Emulation Bus. U51 pin 1, U67 and U54 pin 6 add wait states which slow down the CPU long enough to compensate for the delays added by all the buffers.

8-30. Read/Write Strobe Circuitry.

8-31. Three Sections of U17 form the read strobe generator. If the multiplexers are pointed toward the emulator (MPX low) and the emulator is reading (LEWRT high), or if the multiplexers are pointed toward the CPU (MPX high) and the CPU is reading (LBWRT high), HREAD will be high and a read is indicated. U33, U34, U35 and parts of U18, U36 and U37 form the write strobe generation circuitry. Depending upon the states of LEBYT and LEBUP, or LEBUP and LUPB, the outputs of U35 will allow generation of either LWRU or LWRL, or both. Depending upon the output of U37 pin 12, writes from the emulator may be prevented. The signals that initiate the write strobes are: CPUWSTB for the CPU, and EMWSTB for the Emulator.

8-32. CPU Emulation Memory Access Circuitry.

8-33. A CPU access is initiated when LMAP1 and LBSEL are low and LBSTM makes a high to low transition (HBSTM also goes high). At this time, two actions are initiated: LMSYN is pulled low and U42 pin 11 makes a high to low transition which starts a circuit timeout action of about 1 ms (U42 - U44). Then, when LBSTB goes low, the CPU access request is initiated (U77 pin 5 goes high). If CNTLA is high, the CPU request will be granted within 40 ns after LMAV goes low. If LMAV never goes low, the access will never be granted, in which case the timeout circuitry will timeout and release the CPU. It will also clear a status bit signifying that the access was never granted. The status bit will remain clear until read, at which time U42 pin 7 and U78 pin 11 will set it again. If the access is granted by LMAV going low or if CNTLA is low, it is allowed to continue by U78 pin 8 going high. Since accesses are granted asynchronously with respect to the synchronous state machine (U80, U95 and U96), the accesses must be synchronized. This is done by the CPU access synchronizer (U64). A discrete negative edge latch is used to reduce the time that the output might be meta-stable. When U64 pin 11 goes low signifying a granted access, U80 pin 10 goes high and starts the state machine in action.

The state machine first turns the multiplexers toward the CPU (U96 pin 5 goes low which causes U93 pin 6 to go high. Two states later, U95 pin 5 goes high which causes the CPUWSTB (U62 pin 11) to go low. At the same time this occurs U96 pin 6 goes low causing U94 pin 11 to go low. This clears the access request (U77 pin 5), clears the CPU holdoff (U77 pin 9), and also clears the timeout oneshot. When the oneshot is cleared, U42 pin 9 makes a low to high transition and clocks a low into U44 pin 2, which does not change it from its stable state. If U42 pin 9 timed out without being cleared, a high would be clocked into U44 pin 2. This would cause U44 pin 5 to go high for 50 ns which would clock a low into the access status register (U44 pin 9). With U95 pin 5 high, MPX stays high and, when two U96 pin 5 goes low two states later, the CPUWSTB will go high. Then, the next state would clock a low into U95 pin 5 causing MPX to go low and stop the state machine. The state machine and all access circuitry is cleared at power on by LBPOP and LBBPOP. U93 pin 5 is used to turn the multiplexers around for loading the Mapper RAMs.

8-34. Emulation Memory Access Circuitry.

8-35. An Emulation Memory access is initiated any time HMAV goes low. The state of CNTLB (U53 pin 2) determines the delay from HMAV (from the Emulation Bus) TCLK (U51 pin 10) going high. If CNTLB is high, HMAV propagates through U53, U52 and U51. If CNTLB is low, HMAV propagates through U56 pin 11, U51 pin 12 and U51 pin 9. U52 provides a 60 ns delay for TCLK to permit the address to propagate through the Mapper RAMs and be valid at the outputs of the buffers. TCLK initiates several actions. First, it clocks the LUSER status bit into U49. If LUSER is low, reads are disabled by U50 pin 13 and writes are disabled by U62 pin 10. If LUSER is high, the access proceeds normally. TCLK also clocks the LGRD status bit into U65. If LGRD is low, LBRK (U54 pin 12) and LMBRKS (U56 pin 2) are pulled low. When LBRK is asserted, it can only be released by performing an ID read. This causes LCLSTA to toggle which clears all of U65. TCLK also initiates the triggering of HREADY (U68 pin 11). The inputs to U66 pins 11 and 12 are gated to allow LEWRT (U50 pin 10) and HWDV (U53 pin 5) to transition either before or after TCLK and still provide the necessary time for a write cycle. When U66 pin 9 is triggered, the output goes low for 125 ns (+ or -5ns) and then goes high again. This causes a low to be clocked into U49 pin 9. HREADY, which went low when U50 pin 1 went high, is then allowed to go high again, signifying that the cycle is completed.

8-36. For certain emulators, HWDV will not go high within 125 ns of TCLK. This would cause this circuitry to react as though a read was performed before the write cycle was one half completed. To prevent this, when HWDV propagates through U53 pins 5 and 6, U66 pin 6 is triggered. This causes U51 pin 4 to go low which in turn presets U49 pin 9. If HREADY has already gone low and back high again, the preceeding circuit action will cause it to again go low. Therefore, when HWDV occurs later than than 125 ns after TCLK, the emulator must be able to tolerate HREADY going high for a period during the cycle. If HWDV goes high before the timeout is complete, HREADY will stay low and U66 pin 9 will be retriggered to start the cycle from that point in time. The gated HWDV is also used to clock LROM into U65 pin 10. If LROM is low and LROMEN is low, LBRK and LMBRK will be pulled low. They must be cleared as described above. LMAV going low again clears both one shots and the LUSERL flip flop. It also presets U49 pin 9 for the next cycle. HWDV also initiates the Emulation Memory Write Strobe, EMWSTB. If LUSERL is high and HWDV goes high, U62 pin 8 will go low. If CNTLC (U27 pin 2) is low, U27 pin 1 will go high and cause EMWSTB (U18 pin 4) to go low and stay low until HWDV goes high and propagates through the circuitry. Then, EMWSTB will go high again. If CNTLC (U53 pin 12) is high, the output of U62 pin 8 will cause U27 pin 4 to go high. This drives U53 pin 11 high causing EMTSTB to go low. At the same time the output of U62 pin 8 propagates through U79 pins 1 and 2 and the U26 50 ns delay line. After this occurs, U27 pin 4 will go low which will return EMWSTB high.

Table 8-1. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term).

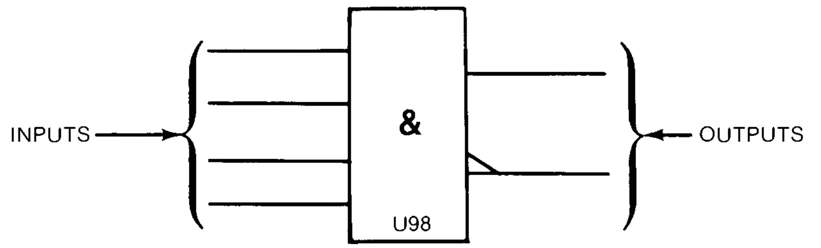
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

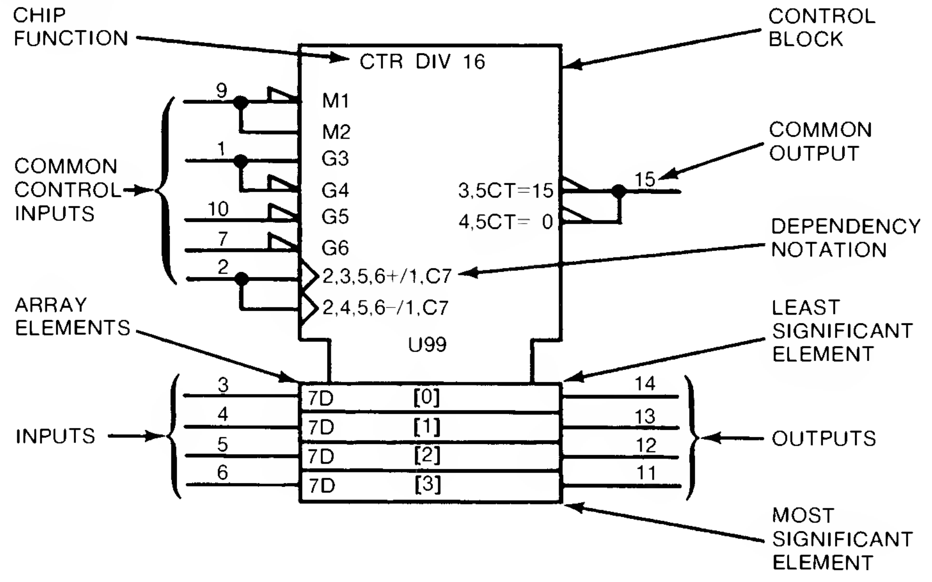
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS - All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. The least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in [ ]).

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection

OTHER SYMBOLS

∩	Analog Signal		Inversion	→	Shift Right (or up)
&	AND	O	Negation	/	Solidus (allows an input or output to have more than one function)
} {	Bit Grouping		Nonlogic Input/Output	▽	Tri-State
▷	Buffer		Open Circuit (NPN) (external resistor)	,	Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
!	Compare		Open Circuit (PNP) (external resistor)	( )	Used for factoring terms using algebraic techniques.
▷	Dynamic	≥1	OR	[ ]	Information not defined.
=1	Exclusive OR		Passive Pull Down (internal resistor)	Φ	Logic symbol not defined due to complexity.
	Hysteresis		Passive Pull Up (internal resistor)		
?	Interrogation		Postponed		
—	Internal Connection	←	Shift Left (or down)		

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	-	Count Down

MATH FUNCTIONS

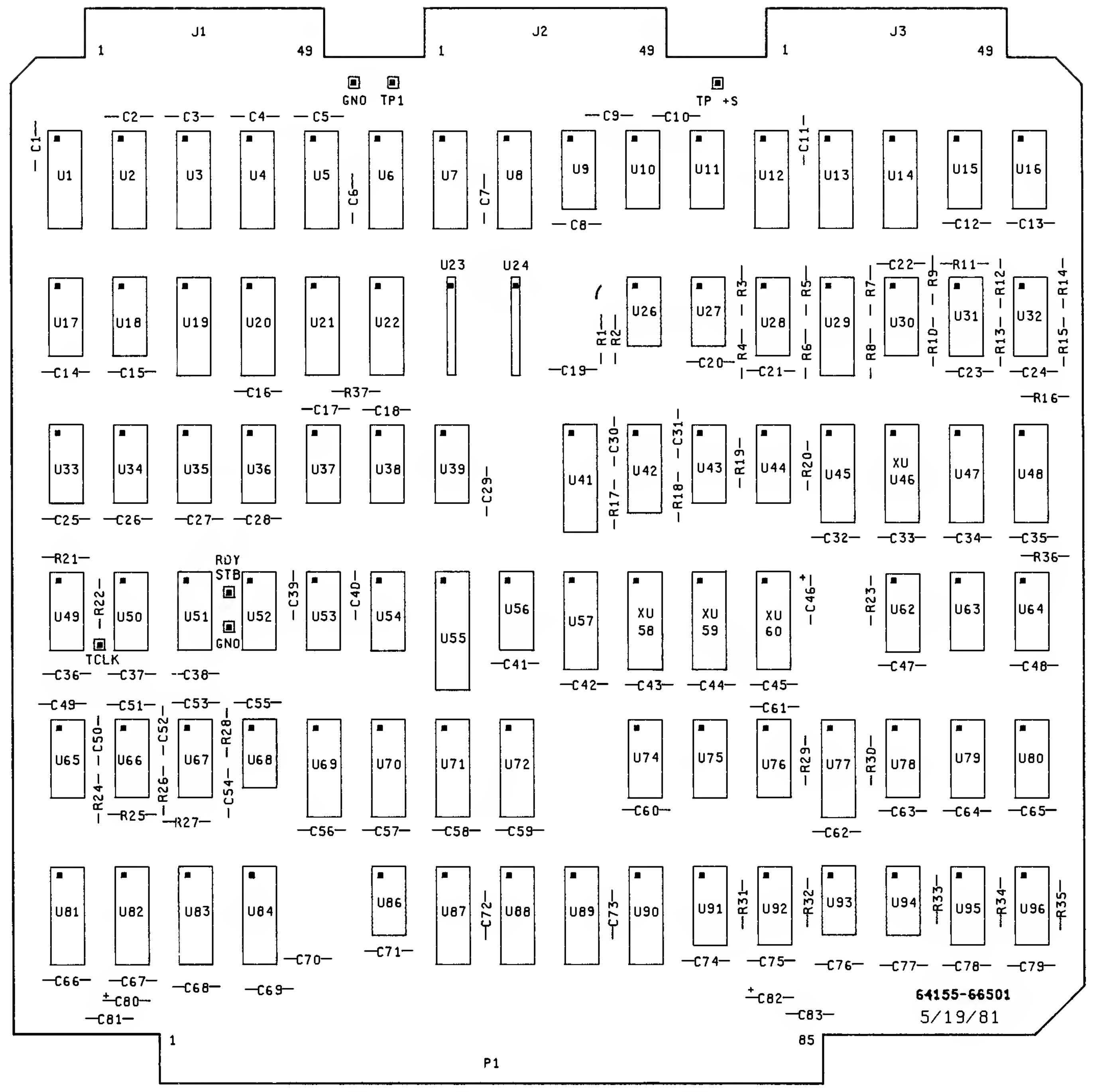
Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	ROM	Read Only Memory
BUF	Buffer	FF	Flip-Flop	RCVR	Line Receiver
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

	Astable
100 ns	Delay
1	Nonretriggerable Monostable
NV	Nonvolatile
	Retriggerable Monostable



Component Locator (64155-66501)

Figure 8-2. 64155A Wide Address Memory Controller

WIDE ADDRESS MEMORY CONTROLLER BLOCK DIAGRAM (64155-66501)

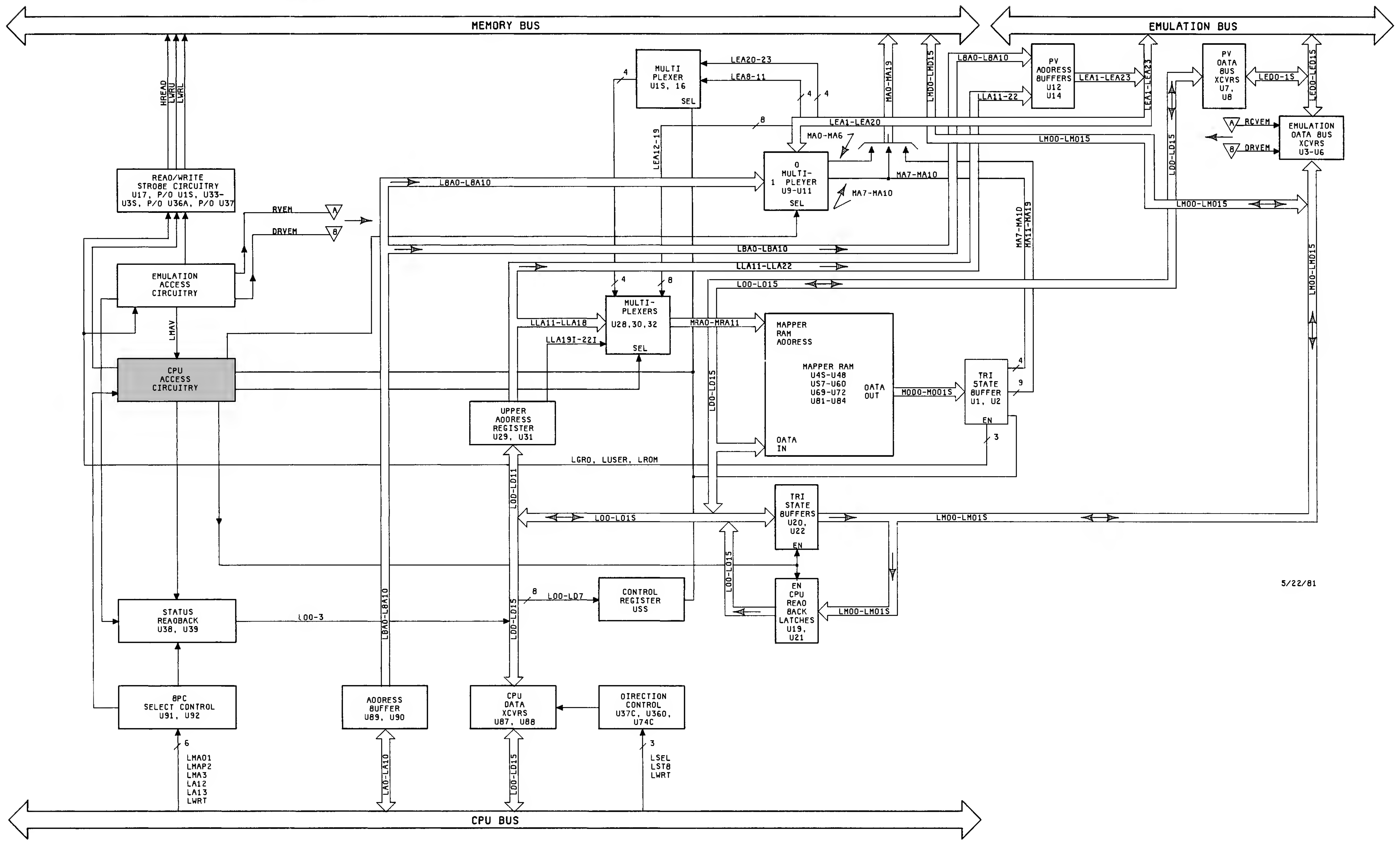
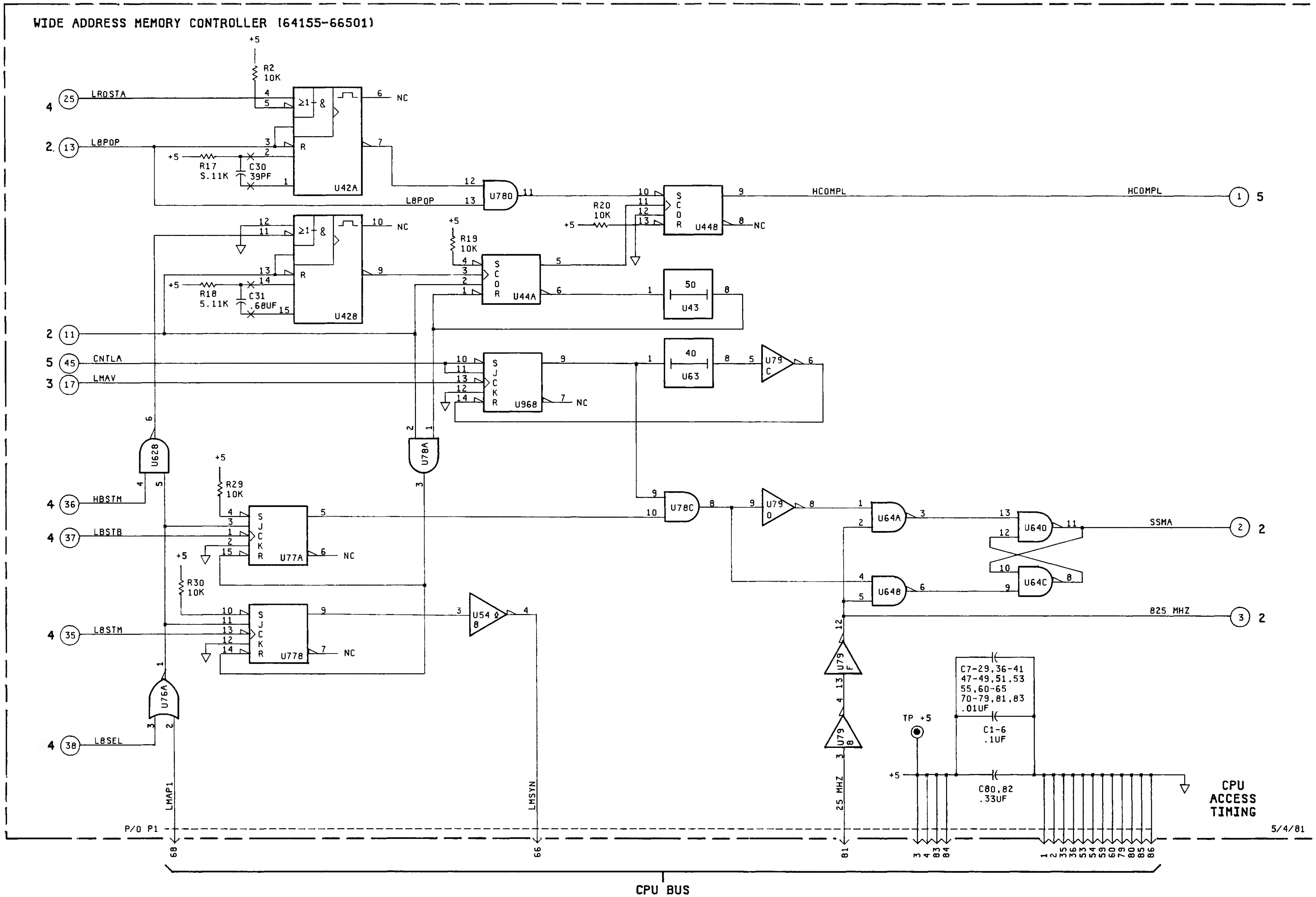


Figure 8-3. CPU Access Timing (Sheet 1 of 2)



1

ICS ON THIS SCHEMATIC

REF DES.	HP PART NO.	MFR.PART NO.
U42	1820-1782	26S02
U43	1820-0555	TTLOL-50
U44	1820-2691	74F74
U54	1820-0684	74S05
U62,64	1820-2684	74F00
U63	1820-0554	TTLOL-40
U76	1820-1144	74LS02N
U77,96	1820-0629	74S112
U78	1820-2686	74F08
U79	1820-2506	74F04

PARTS ON THIS SCHEMATIC

C1-31,36-41,47-49,51,53,55
60-65,70-83
R2,17-20,29,30
TP+5,GNO
U42-44,54,62-64
76-79,96

POWER SUPPLY CONFIGURATIONS

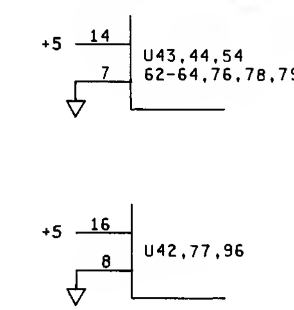


Figure 8-3.
CPU Access Timing (Sheet 2 of 2)

WIDE ADDRESS MEMORY CONTROLLER BLOCK DIAGRAM (64155-66501)

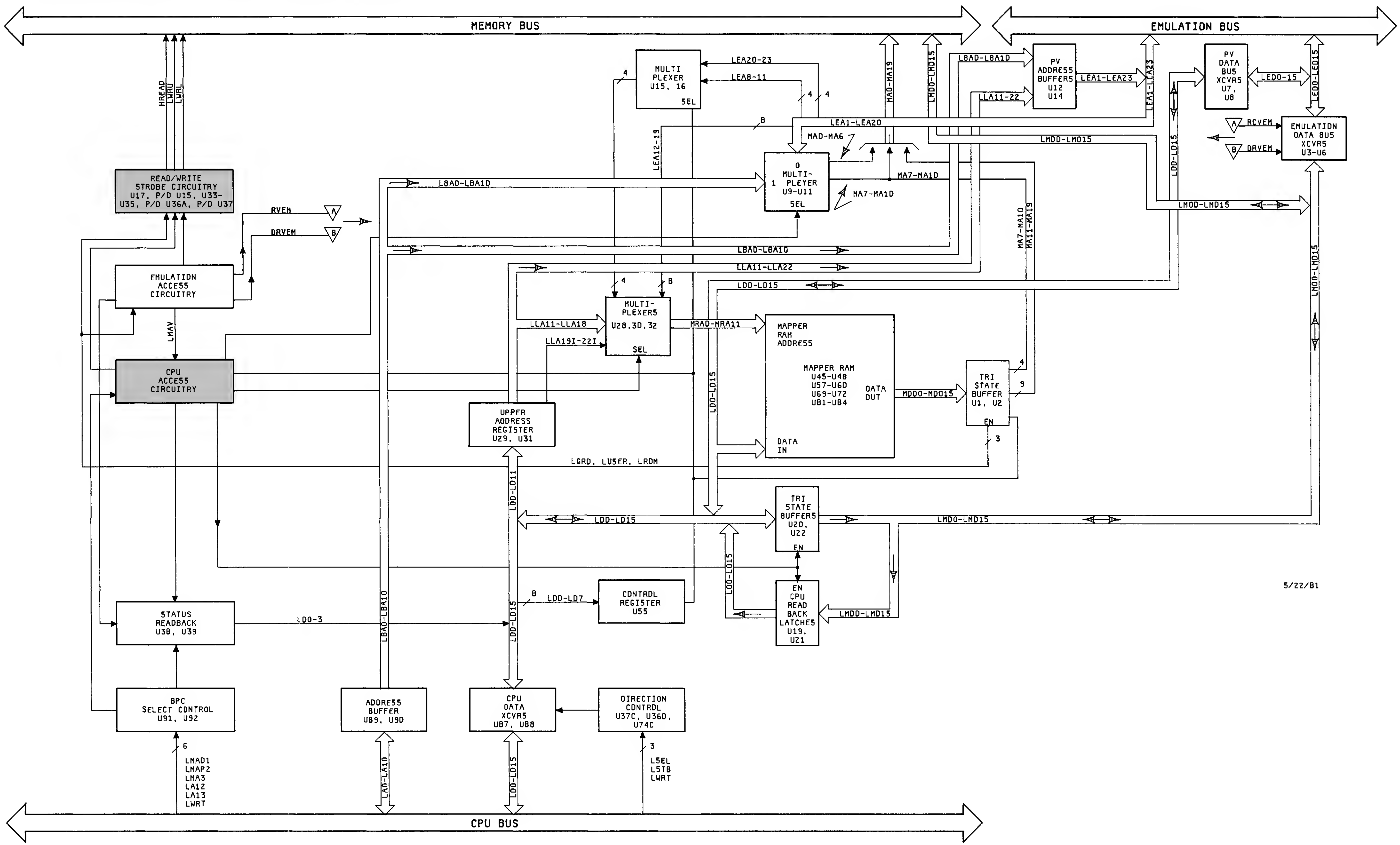
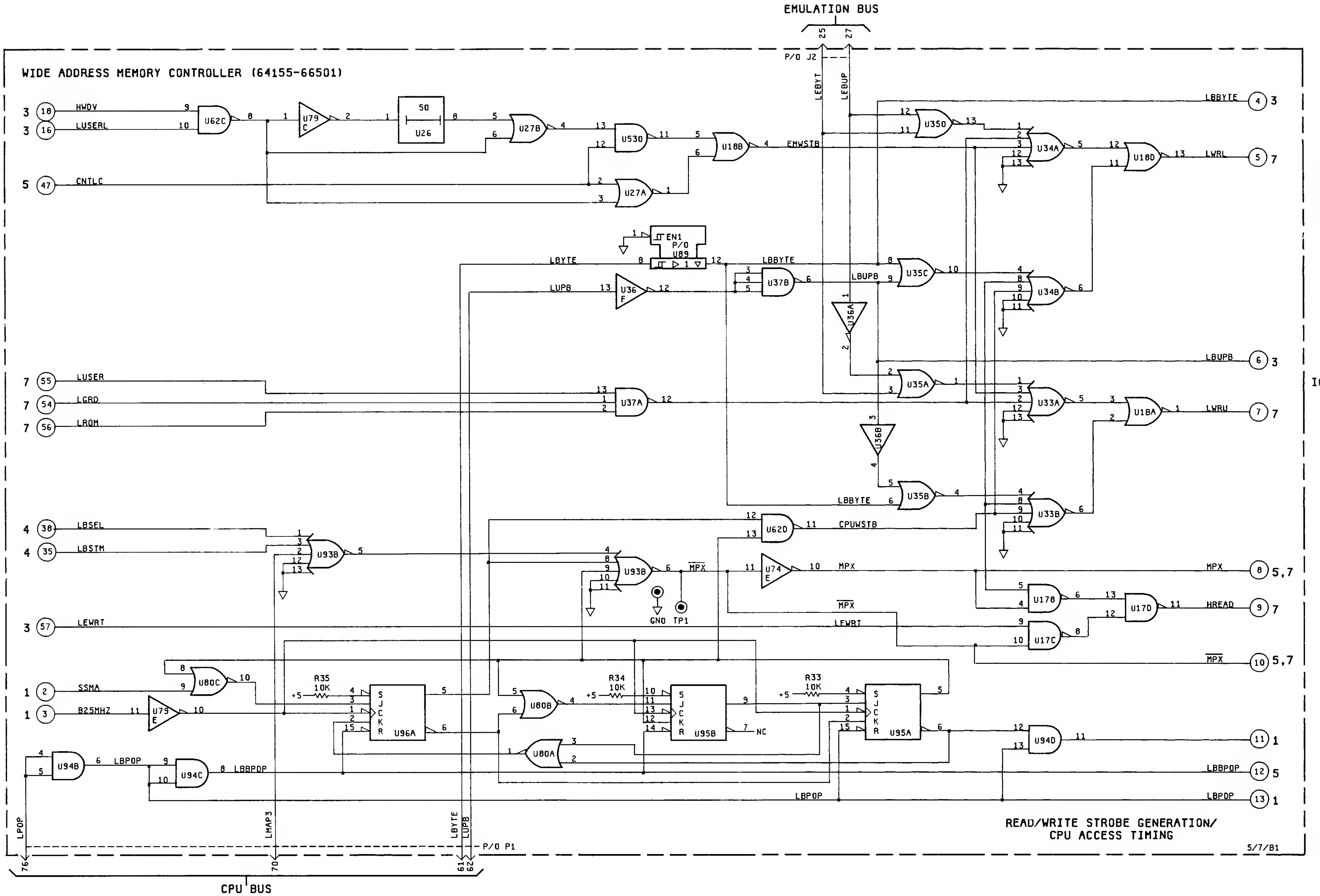


Figure 8-4. CPU Access Timing and Read/Write Strobe Generation (Sheet 1 of 2)



ICS ON THIS SCHEMATIC

REF.DES.	HP PART NO.	MFR PART NO.
U17,62	1820-2684	74F00
U18,27, 35,80	1820-2685	74F02
U26	1820-0555	TTLDL-50
U29	1820-1997	74LS374
U33,34, 93	1820-1275	74S260
U36,74, 79	1820-2506	74F04
U37	1820-2687	74F10
U53,94	1820-2686	74F08
U89	1820-2024	74LS244
U95,96	1820-0629	74S112

PARTS ON THIS SCHEMATIC

R33-35
TP1,GND
U17,18,26,27,29,33-37,53,62,74,79,80,93-96

IC POWER SUPPLY CONFIGURATIONS

+5 14 7 U17,18,26,27, 33-37,53,74, 79,80,93,94

+5 20 10 U29,89

+5 16 8 U95,96

Figure 8-4.
CPU Access Timing and Read/Write Strobe Generation
(Sheet 2 of 2)

WIDE ADDRESS MEMORY CONTROLLER BLOCK DIAGRAM (64155-66501)

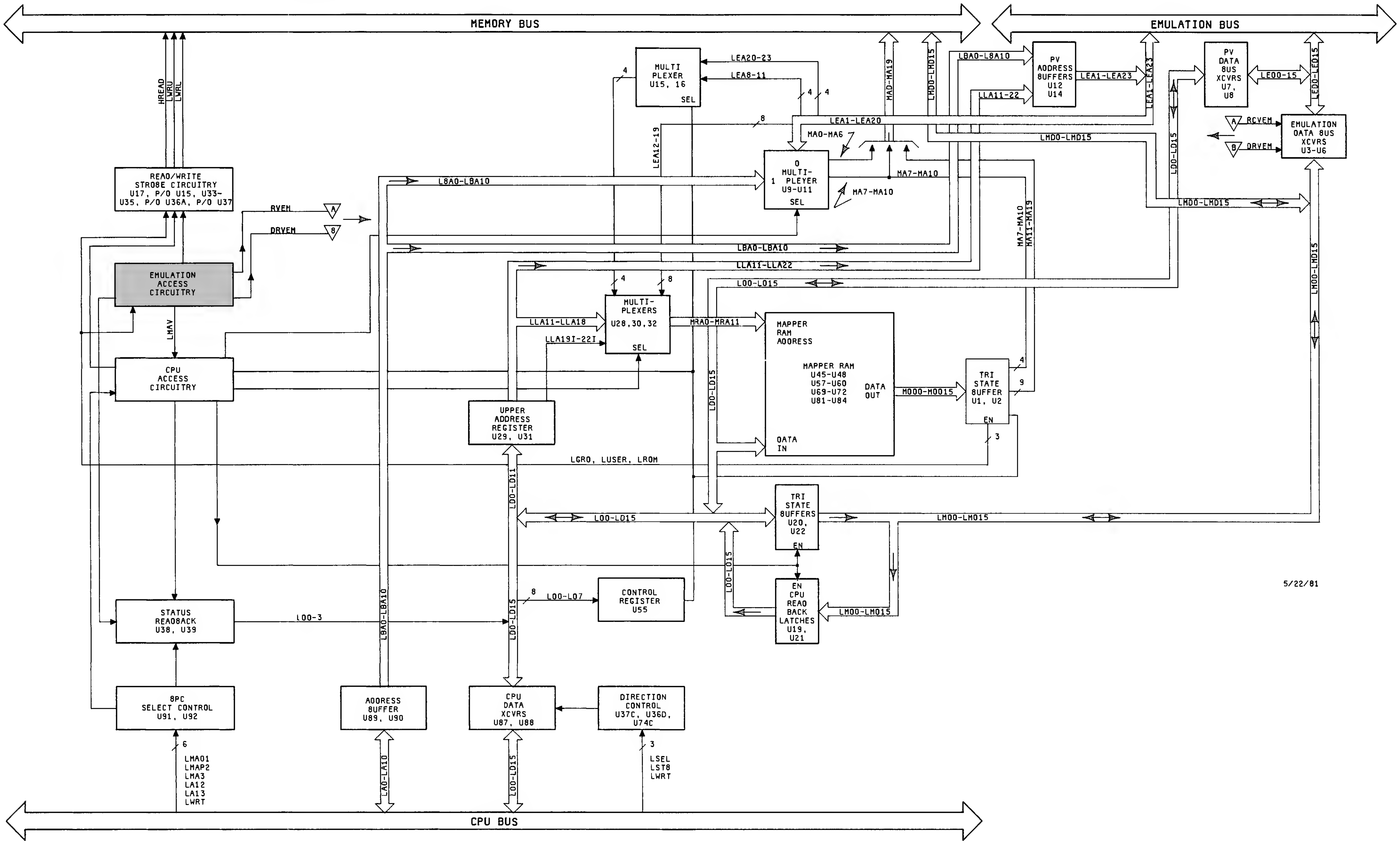
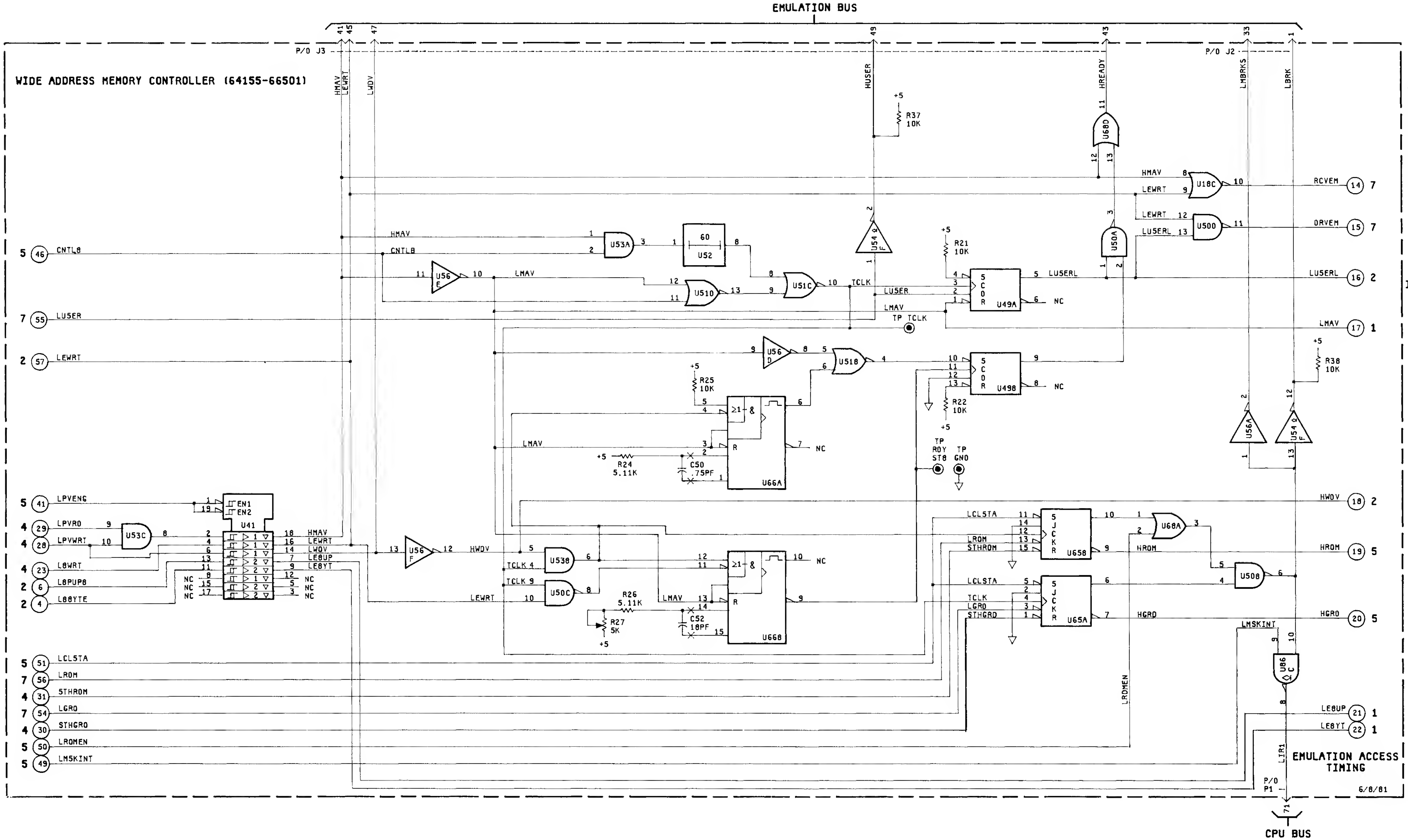


Figure 8-5. Emulation Access Timing (Sheet 1 of 2)



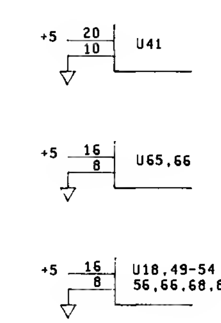
ICS ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U18,51	1820-2685	74F02
U41	1820-2024	74LS244
U49	1820-2691	74F74
U50	1820-2684	74F00
U52	1820-0556	TTDL-60
U53	1820-2686	74F08
U54	1820-0684	74S05
U56	1820-2506	74S04
U65	1820-2693	74F109
U66	1820-1782	26S02
U68	1820-2690	74F32
U86	1820-0682	74S03

PARTS ON THIS SCHEMATIC

C50,52
R21,22,24-27,37,38
TP-TCLK,RDY STB,GND
U18,41,49-54,56,65,66,68,86

IC POWER SUPPLY CONFIGURATIONS



WIDE ADDRESS MEMORY CONTROLLER BLOCK DIAGRAM (64155-66501)

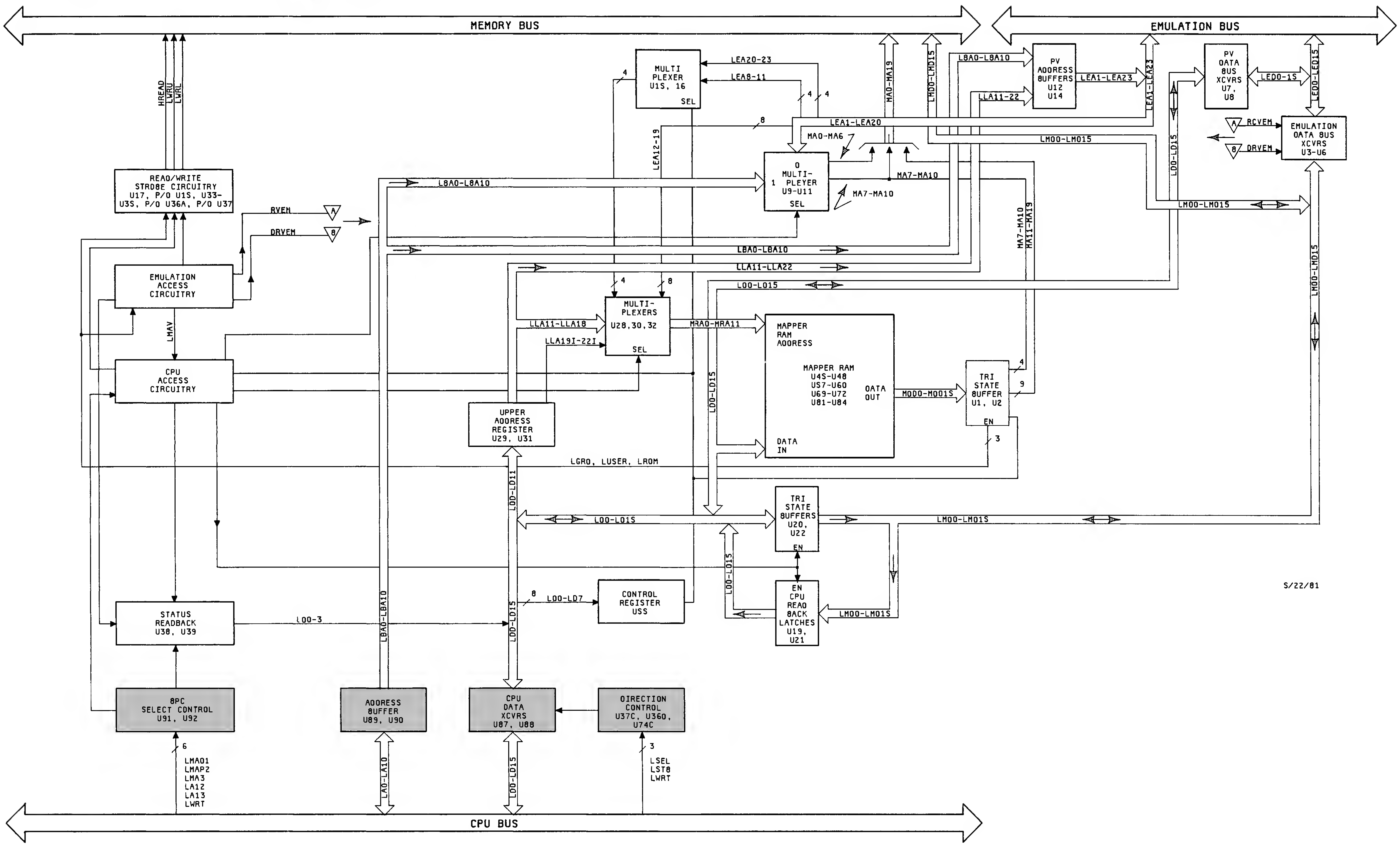
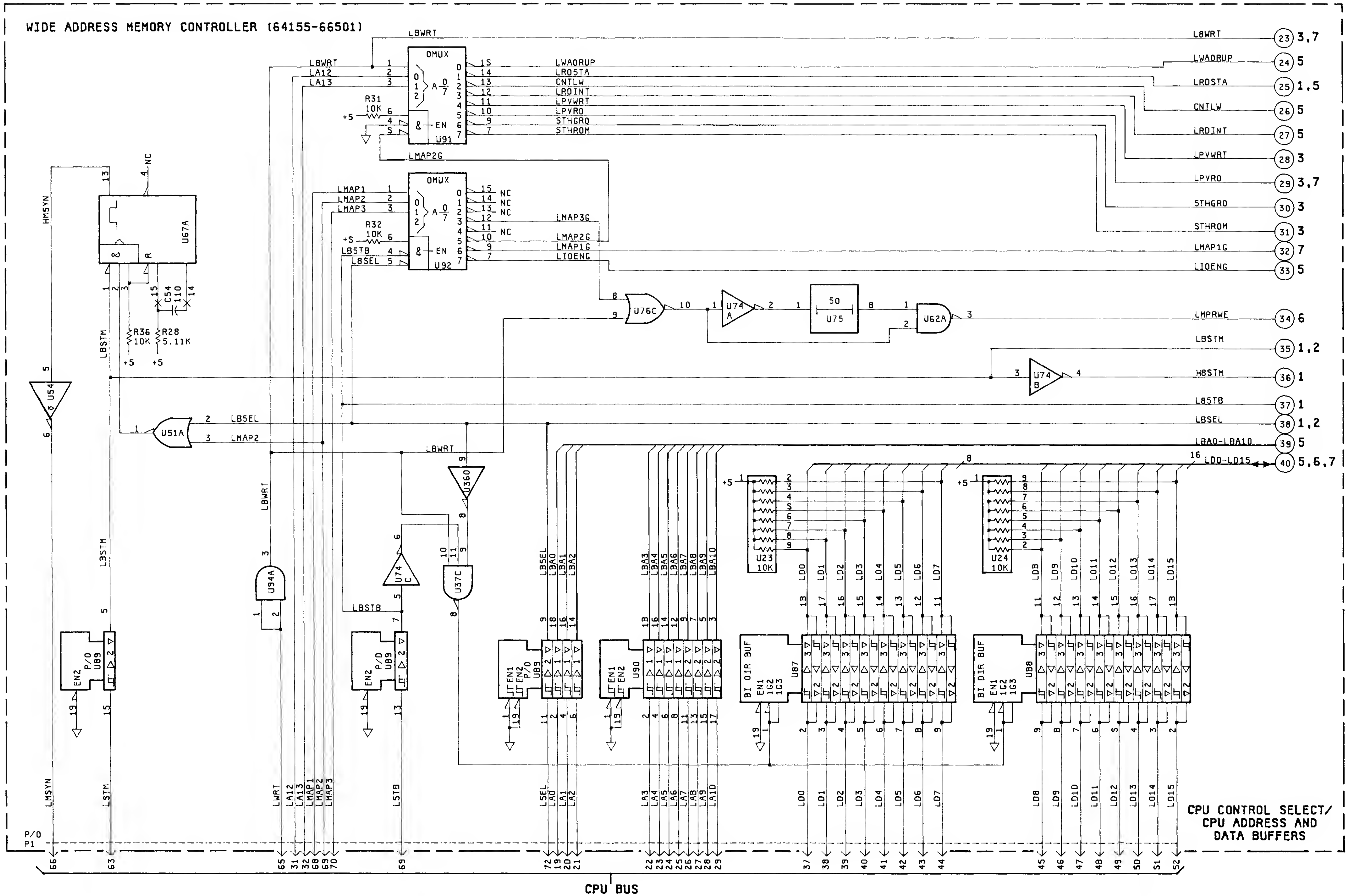


Figure 8-6. CPU Control Select and CPU Address and Data Buffers (Sheet 1 of 2)



ICS ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFR. PART NO.
U23,24	1810-0280	210A103
U36,74	1820-2S06	74F04
U37	1820-2687	74F10
U51	1820-2685	74F02
U54	1820-0684	74S05
U62	1820-2684	74F00
U67	1820-1423	74LS123
U75	1810-0S55	TTLDL-S0
U76	1820-1144	74LS02
U87,88	1820-2075	74LS245
U89,90	1820-2024	74LS244
U91,92	1820-1216	74LS138
U94	1820-2686	74F08

PARTS ON THIS SCHEMATIC

CS4
R28,31,32,36
U23,24,36,37,51,54,62,67,74-76,
87-92,94

IC POWER SUPPLY CONFIGURATIONS

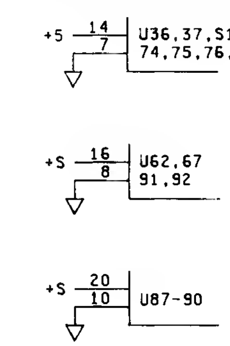


Figure 8-6.
CPU Control Select and CPU Address and Data Buffers
(Sheet 2 of 2)

WIDE ADDRESS MEMORY CONTROLLER BLOCK DIAGRAM (64155-66501)

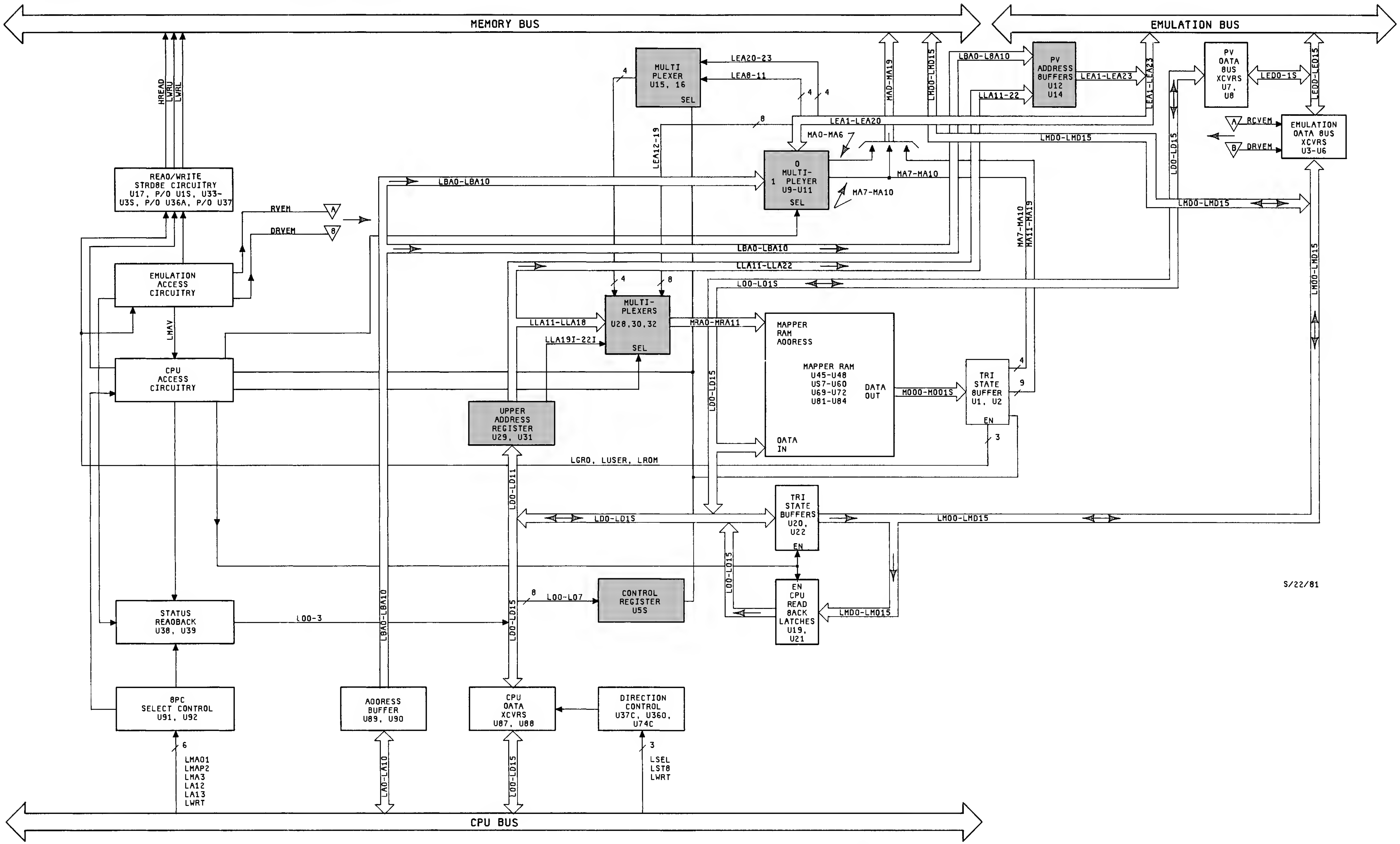
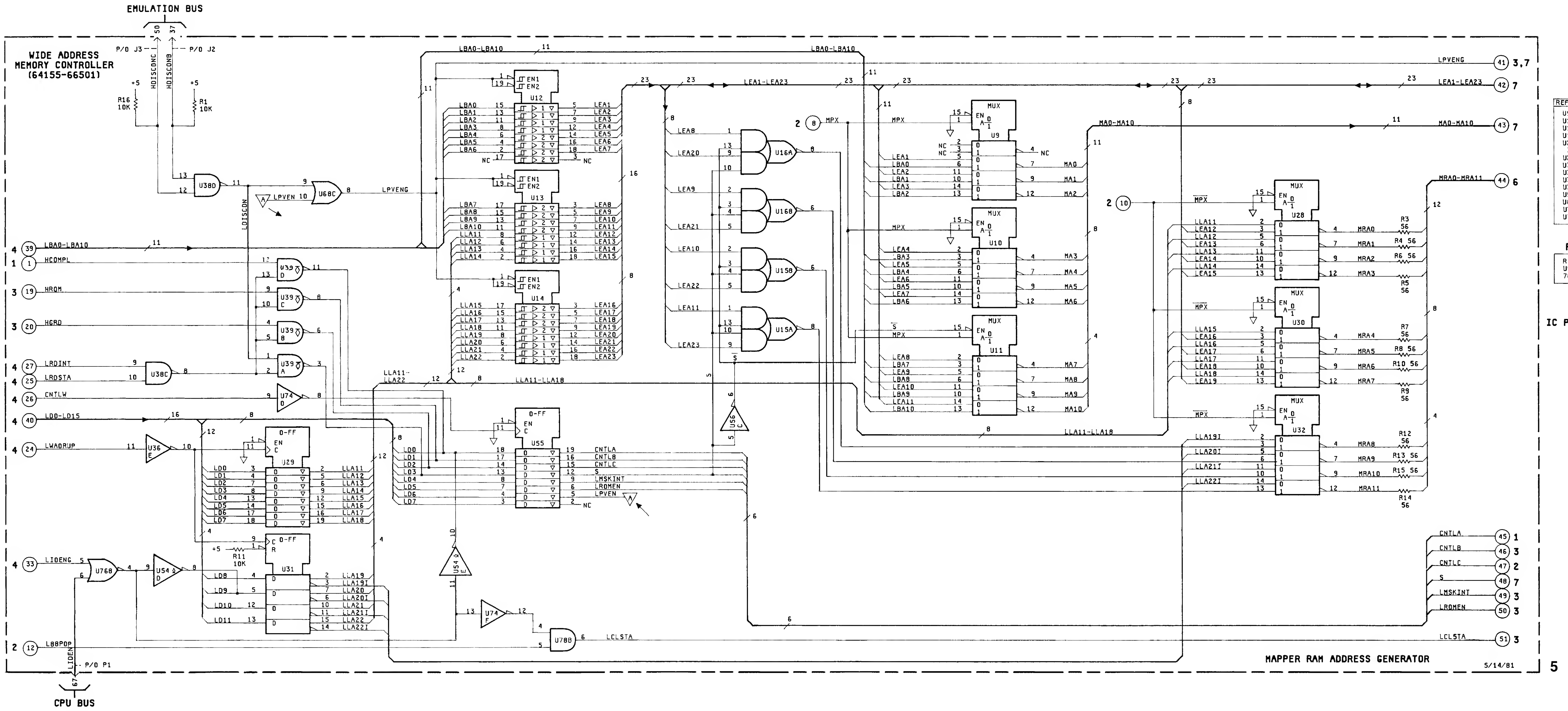


Figure 8-7. Mapper RAM Address Generator and Memory Address Specifier (Sheet 1 of 2)



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U11	1820-1439	74LS258
U12-14	1820-2024	74LS244
U15,16	1820-1158	74S51
U28,30, 32	1820-2695	74F158
U29,55	1820-1997	74LS374
U31	1820-1195	74LS175
U36,74	1820-2506	74F04
U38	1820-1197	74LS00
U39	1820-1198	74LS03
U54	1820-0684	74S05
U68	1820-1449	74S32
U76	1820-1144	74LS02
U78	1820-2686	74F08

PARTS ON THIS SCHEMATIC

R1,3-16
U9-16,28-32,36,38,39,53,54,68,74,76,78

IC POWER SUPPLY CONFIGURATIONS

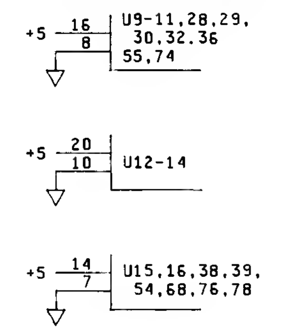


Figure 8-7.
Mapper RAM Address Generator and Memory Address Specifier
(Sheet 2 of 2)

WIDE ADDRESS MEMORY CONTROLLER BLOCK DIAGRAM (64155-66501)

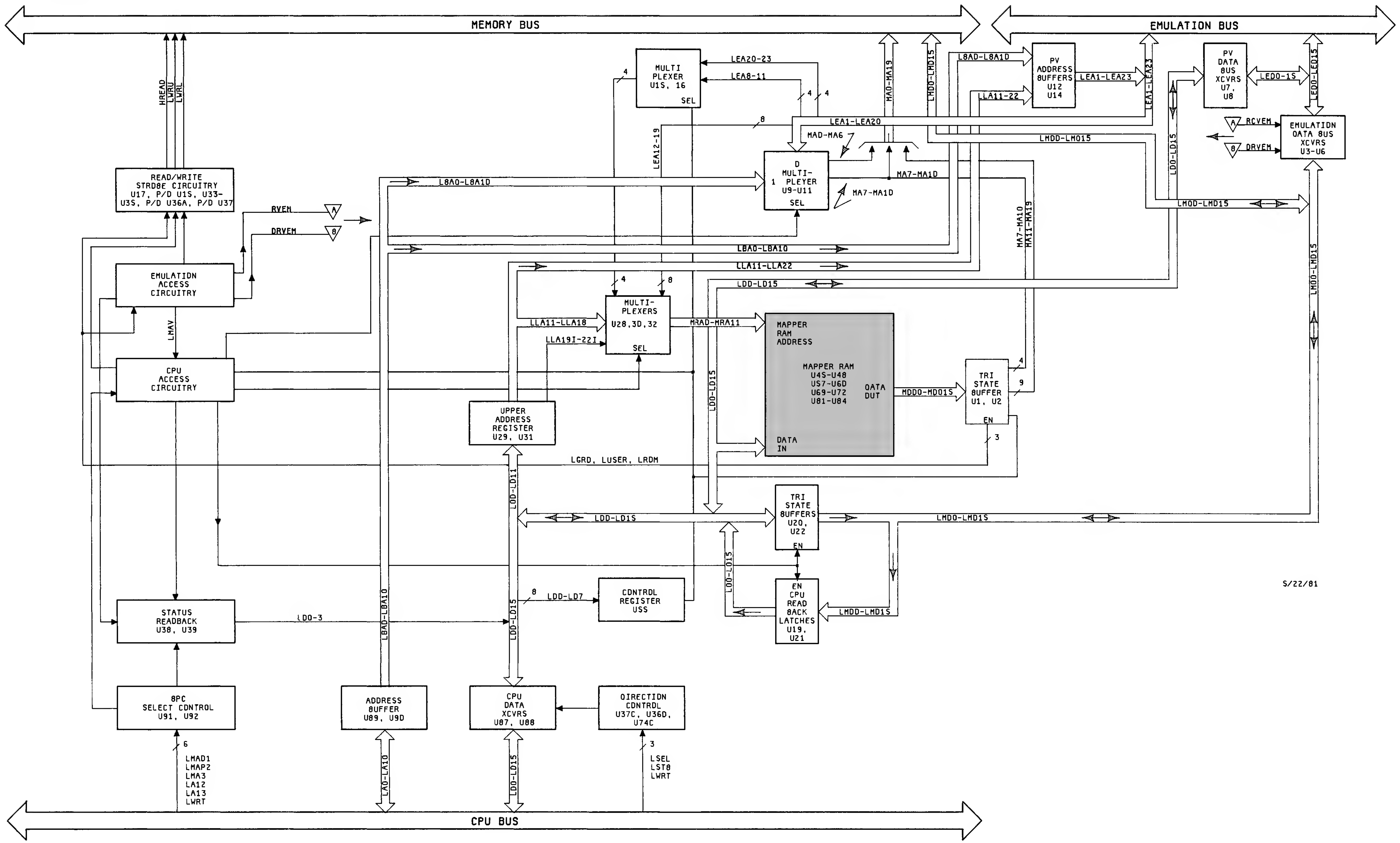
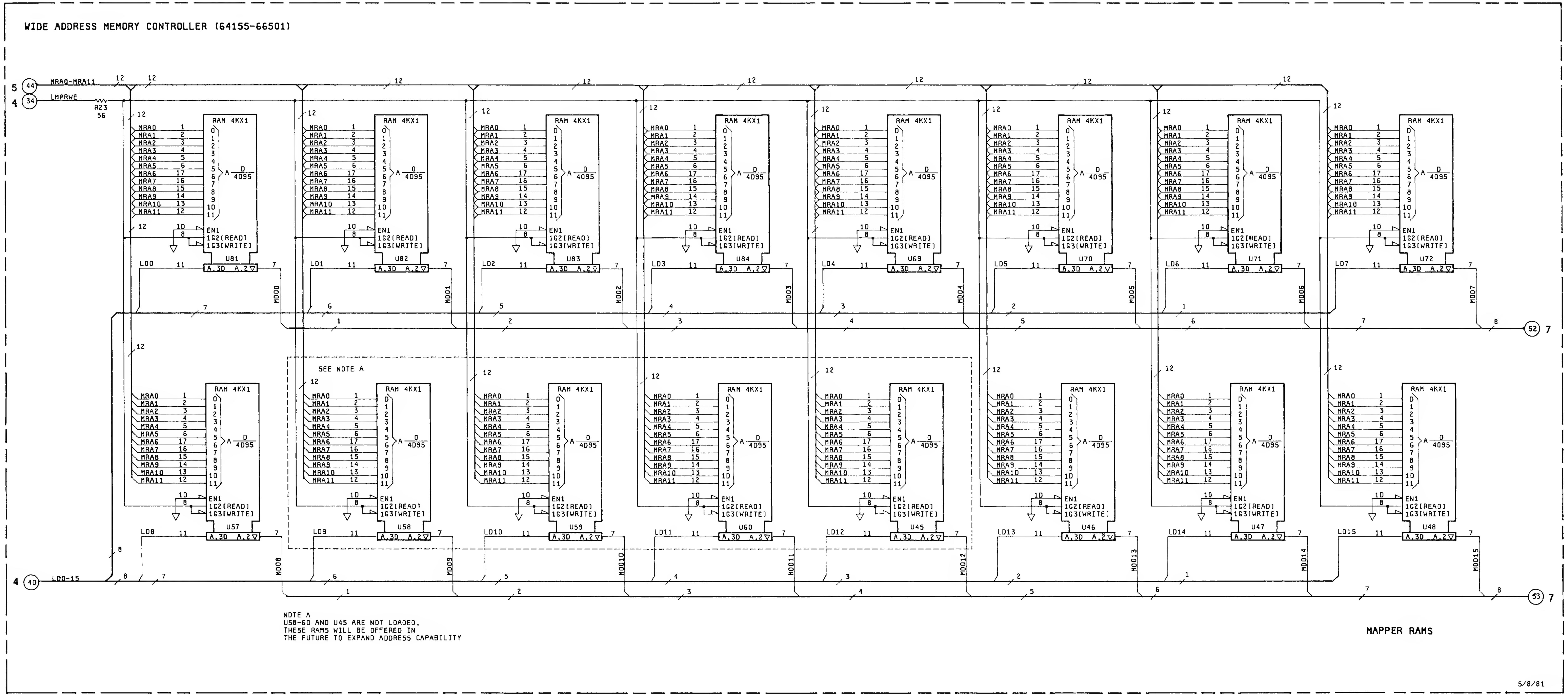


Figure 8-8. Mapper RAMs (Sheet 1 of 2)



ICS ON THIS SCHEMATIC

REF. DES.	MFR. PART NO.	HP PART NO.
U45 58-60		SEE NOTE A
U46-48, 57, 69-72, 81-84	1818-1586	2147H-1

PARTS ON THIS SCHEMATIC

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R23
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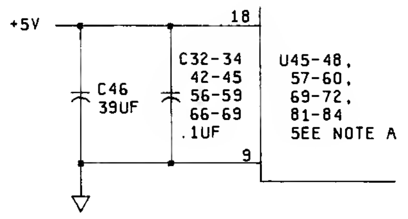

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Figure 8-8.
Mapper RAMs (Sheet 2 of 2)

WIDE ADDRESS MEMORY CONTROLLER BLOCK DIAGRAM (64155-66501)

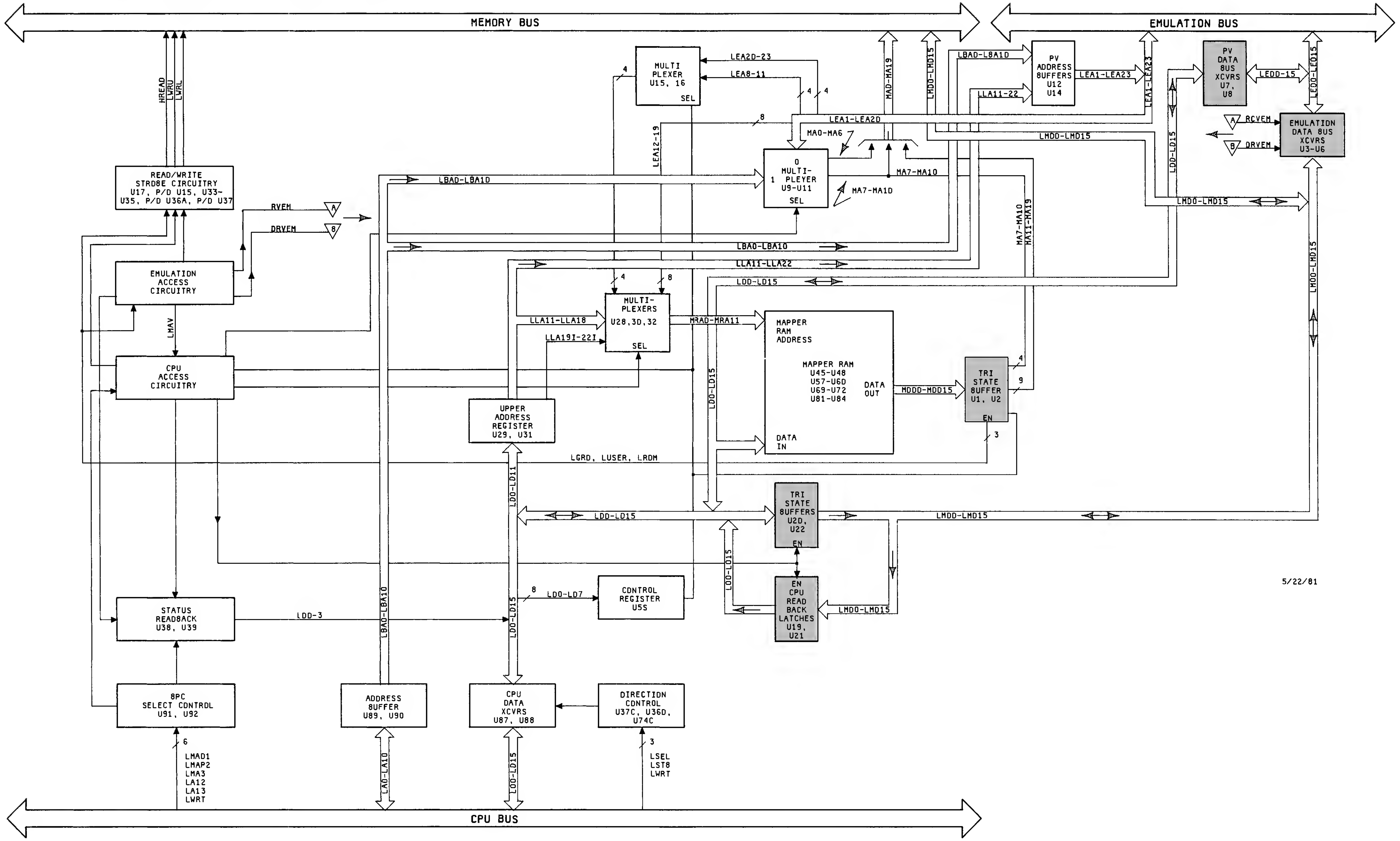
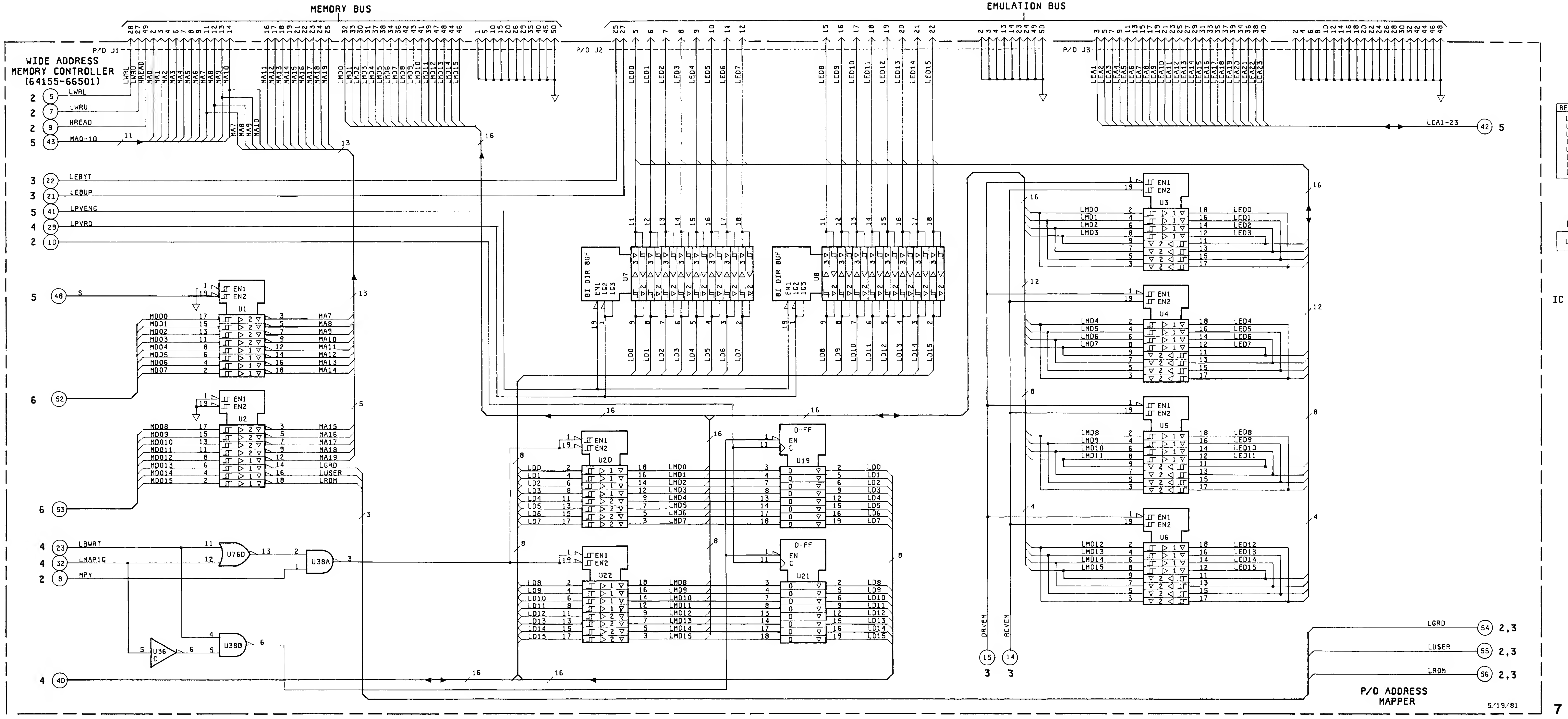


Figure 8-9. Address Mapper (Sheet 1 of 2)



ICS ON THIS SCHEMATIC

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U7,8	1820-2075	74LS245
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U20,22	1820-2024	74LS244
U36	1820-2506	74F04
U38	1820-1197	74LS00
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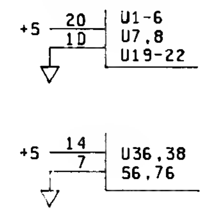

Figure 8-9.
Address Mapper (Sheet 2 of 2)

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3. The information in this book is easy to find:

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5. What about the "how-to" procedures and examples:

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Telex: 361157
CH,M

Hewlett-Packard France
13, Place Napoleon III
F-29000 **BREST**
Tel: (98) 03-38-35

Hewlett-Packard France
Chemin des Mouilles
Boite Postale 162
F-69130 **ECULLY** Cedex (Lyon)
Tel: (78) 833-81-25
Telex: 310617F
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Hewlett-Packard France
Parc d'Activite du Bois Briard
Ave. du Lac
F-91040 **EVRY** Cedex
Tel: 6 077-8383
Telex: 692315F
E

Hewlett-Packard France
5, Avenue Raymond Chanas
F-38320 **EYBENS** (Grenoble)
Tel: (76) 62-67-98
Telex: 980124 HP GRENOB EYBE
CH

Hewlett-Packard France
Centre d'Affaire Paris-Nord
Bâtiment Ampère 5 étage
Rue de la Commune de Paris
Boite Postale 300
F-93153 **LE BLANC MESNIL**
Tel: (1) 865-44-52
Telex: 211032F
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Hewlett-Packard France
Parc d'Activités Cadera
Quartier Jean Mermoz
Avenue du Président JF Kennedy
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Telex: 550105F
CH,E,M

Hewlett-Packard France
Immueble "Les 3 B"
Nouveau Chemin de la Garde
ZAC de Bois Briand
F-44085 **NANTES** Cedex
Tel: (40) 50-32-22
Telex: 711085F
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125, rue du Faubourg Bannier
F-45000 **ORLEANS**
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Avenue des Tropiques
F-91947 Les Ulis Cedex **ORSAY**
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F-75782 **PARIS** CEDEX 16
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F-64000 **PAU**
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F-35100 **RENNES**
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F-76100 **ROUEN**
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Telex: 770035F
CH**,CS

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F-26000 **VALENCE**
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Hewlett-Packard France
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F-57640 **VIGY** (Metz)
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CH

Hewlett-Packard France
Immeuble PEricentre
F-59658 **VILLENEUVE D'ASCQ** Cedex
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Hewlett-Packard GmbH
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Keithstrasse 2-4
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Hewlett-Packard GmbH
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Vertriebszentrale Frankfurt
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Hewlett-Packard GmbH
Geschäftsstelle
Aussenstelle Bad Homburg
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Hewlett-Packard GmbH
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Hewlett-Packard GmbH
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A,CH,CM,E,M,P

GREAT BRITAIN
See United Kingdom

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Arranged alphabetically by country

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Hewlett-Packard A.E.
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Halandri-**ATHENS**
Greece
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A,CH,CM**,CS**,E,M,P

Kostas Karaynnis S.A.
8 Omirou Street
***ATHENS** 133*
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Telex: 215962 RKAR GR
A,CH,CM,CS,E,M,P

PLAISIO S.A.
Eliopoulos Brohers Ltd.
11854
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Telex: 216286
P

GUATEMALA
IPESA
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GUATEMALA CITY
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E,CH,CS,P

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64-66 Gloulester Road
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Telex: 85148 CET HX
CM

Schmidt & Co. (Hong Kong) Ltd.
18th Floor, Great Eagle Centre
23 Harbour Road, Wanchai
HONG KONG
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A,M

ICELAND
Elding Trading Company Inc.
Hafnarnvoli-Tryggvagotu
P.O. Box 895
IS-REYKJAVIK
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M

INDIA
Computer products are sold through Blue Star Ltd.All computer repairs and maintenance service is done through Computer Maintenance Corp.

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Sabri Complex II Floor
24 Residency Rd.
BANGALORE *560 025*
Tel: 55660
Telex: 0845-430
Cable: BLUESTAR
A,CH,CM,CS*,E*

Blue Star Ltd.
Band Box House
Prabhadevi
BOMBAY *400 025*
Tel: 422-3101
Telex: 011-3751
Cable: BLUESTAR
A,M

Blue Star Ltd.
Sahas
414/2 Vir Savarkar Marg
Prabhadevi
BOMBAY *400 025*
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Telex: 011-71193
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Alkapuri, **BORODA,** *390 005*
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***CALCUTTA** 700 001*
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Cable: BLUESTAR
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Cable: BLUESTAR
A,M

Blue Star Ltd.
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NEW DELHI *110 024*
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Telex: 031-2463
Cable: BLUESTAR
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Blue Star Ltd.
15/16:C Wellesley Rd.
PUNE *411 011*
Tel: 22775
Cable: BLUE STAR
A

Blue Star Ltd.
2-2-47/1108 Bolarum Rd.
SECUNDERABAD *500 003*
Tel: 72057
Telex: 0155-459
Cable: BLUEFROST
A,E

Blue Star Ltd.
T.C. 7/603 Poornima
Maruthankuzhi
TRIVANDRUM *695 013*
Tel: 65799
Telex: 0884-259
Cable: BLUESTAR
E

Computer Maintenance Corporation Ltd.
115, Sarojini Devi Road
SECUNDERABAD *500 003*
Tel: 310-184, 345-774
Telex: 031-2960
*CH***

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BERCA Indonesia P.T.
P.O.Box 496/Jkt.
Jl. Abdul Muis 62
JAKARTA
Tel: 21-373009
Telex: 46748 BERSAL IA
Cable: BERSAL JAKARTA
P

BERCA Indonesia P.T.
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Antara Bldg., 17th Floor
Jl. Medan Merdeka Selatan 17
JAKARTA-PUSAT
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Telex: BERSAL IA
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P.O. Box 174/SBY.
Jl. Kutei No. 11
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Telex: 31146 BERSAL SB
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Service Operation
Al Mansoor City 9B/3/7
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Telex: 212-455 HEPAIRAQ IK
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Hewlett-Packard Ireland Ltd.
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Telex: 30439
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Cardiac Services Ltd.
Kilmore Road
Artane
DUBLIN *5*
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Telex: 30439
M

ISRAEL
Eldan Electronic Instrument Ltd.
P.O.Box 1270
JERUSALEM *91000*
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Telex: 25231 AB/PAKRD IL
A,M

Computation and Measurement
Systems (CMS) Ltd.
11 Masad Street
67060
TEL-AVIV
Tel: 388 388
Telex: 33569 Motil IL
CH,CM,CS,E,P

ITALY
Hewlett-Packard Italiana S.p.A
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M,CH

Hewlett-Packard Italiana S.p.A.
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I-40132 **BOLOGNA**
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CH,CS,E,M

Hewlett-Packard Italiana S.p.A.
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I-95126 **CATANIA**
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Telex: 970291
CH

Hewlett-Packard Italiana S.p.A.
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I-20063 **CERNUSCO SUL NAVIGLIO**
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Hewlett-Packard Italiana S.p.A.
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I-20090 **TREZZANO SUL NAVIGLIO**
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A**,CH,CS,E,M

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I-16156 **GENOVA PEGLI**
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I-35128 **PADOVA**
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I-10144 **TORINO**
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CM,C*,E

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CHIBA, 280
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E,CH,CS

Yokogawa-Hewlett-Packard Ltd.
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C,E

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CH,E

Yokogawa-Hewlett-Packard Ltd.
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Notabile Rd.
MRIEHEL
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E,P,M

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Colonia del Valle
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GUADALAJARA
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Despacho 2001
Colonia Del Valle
MONTERREY
Tel: 782499, 781259A
A

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Telex: 23051, 22822
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Gerep
2 rue d'Agadir
Boite Postale 156
CASABLANCA
Tel: 272093, 272095
Telex: 23 739
P

Sema-Maroc
Rue Lapebie
CASABLANCA
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NL1180 AR **AMSTELVEEN**
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Telex: 13 216 HEPA NL
A,CH,CM,CS,E,M,P

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Bongerd 2
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P.O. Box 41
NL 2900AA **CAPELLE A/D IJSSEL**
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Telex: 21261 HEPAC NL
A,CH,CS,E

Hewlett-Packard Nederland B.V.
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NL 5612 LV **EINDHOVEN**
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NL 5600 CH **EINDHOVEN**
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A,CH**,E,M

SALES & SUPPORT OFFICES
Arranged alphabetically by country

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CH,CS,CM,E,P*

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Courtenay Place, **WELLINGTON 3**
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Cable: HEWPACK Wellington
CH,CS,CM,E,P

Northrop Instruments & Systems Ltd.
369 Khyber Pass Road
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AUCKLAND
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Telex: 60605
A,M

Northrop Instruments & Systems Ltd.
110 Mandeville St.
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CHRISTCHURCH
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Telex: 4203
A,M

Northrop Instruments & Systems Ltd.
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A,M

NORTHERN IRELAND
See United Kingdom

NORWAY
Hewlett-Packard Norge A/S
Folke Bernadottes vei 50
P.O. Box 3558
N-5033 **FYLLINGSDALEN** (Bergen)
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CH,CS,E,M

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UCOsterndalen 16-18
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A,CH,CM,CS,E,M,P

OMAN
Khimjil Ramdas
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Tel: 722225, 745601
Telex: 3289 BROKER MB MUSCAT
P

Suhail & Saud Bahwan
P.O.Box 169
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Tel: 734 201-3
Telex: 3274 BAHWAN MB
E

Imtac LLC
P.O. Box 8676
MUTRAH
Tel: 601695
Telex: 5741 Tawoos On
A,C,M

PAKISTAN
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*A,E,M,P**

Mushko & Company Ltd.
Oosman Chambers
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Tel: 524131, 524132
Telex: 2894 MUSKO PK
Cable: COOPERATOR Karachi
*A,E,M,P**

PANAMA
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Calle Samuel Lewis, Ed. Alfa
Apartado 4929
PANAMA *5*
Tel: 63-6613, 63-6748
Telex: 3483 ELECTRON PG
A,CM,E,M,P

PERU
Cía Electro Médica S.A.
Los Flamencos 145, San Isidro
Casilla 1030
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